Performance of Thin-Film Transistors with Ultrathin Ni-MILC Polycrystalline Silicon Channel Layers

Zhonghe Jin, Hoi S. Kwok, and Man Wong

***Abstract*—High-performance, low-temperature processed thin-film transistors (TFT's) with ultrathin (30-nm) metal induced laterally crystallized (MILC) channel layers were fabricated and characterized. Compared with the MILC TFT's with thicker (100 nm) channel layers, the ones with the 30-nm channel layers exhibit lower threshold voltage, steeper subthreshold slope, and higher transconductance. Furthermore, the comparatively lower off-state leakage current and the higher on-state current of the "thin" devices also imply a higher on/off ratio. At a drain voltage of 5 V, an on/off ratio of about 3×10^7 was obtained for the 30-nm TFT's, which is about 100 times better than that of the 100-nm TFT's. No deliberate hydrogenation was performed on these devices.**

***Index Terms*—Displays, MILC, nickel, thin-film transistors.**

I. INTRODUCTION

SILICON-ON-INSULATOR (SOI) metal–oxide–semiconductor field-effect transistors (MOSFET's) with ultrathin channel layers have various advantages. These include high mobility [1], kink elimination [2], saturation current enhancement [3], and steeper subthreshold slope (S). Similar beneficial effects have also been observed [4] in polycrystalline silicon (poly-Si) TFT's with thin channel layers. Little *et al.* [5] successfully fabricated low-temperature poly-Si TFT's with 25-nm thick channels by solid phase crystallization (SPC). However, the field effect mobility $(\mu_{\rm FE})$ of the device is less than 25 cm^2/Vs, mainly due to a significant reduction of the lateral grain size with the film thickness. Employing suitably optimized Excimer laser crystallization (ELC), Kuriyama *et al.* [6] realized larger lateral grain size in ultrathin silicon film and fabricated better performing TFT's with 50-nm thick channel layers—achieving a $\mu_{\rm FE}$ as high as 280 cm^2/Vs and an on/off ratio above 10^6.

MILC, a technique more compatible with batch processing than ELC, is recently developed for the realization of TFT's [7]. Whereas the lateral grain size formed using SPC reduces with the thickness of the amorphous silicon (a-Si) layer, poly-Si films with large lateral grain sizes independent of the film thickness can be formed using MILC [8]. Consequently, MILC-TFT's with 30-nm thick channel layers are demonstrated in this work to have better performance that similar TFT's with 100-nm thick channel layers.

Manuscript received September 27, 1998; revised October 19, 1998. This work was supported by a Competitive Earmarked Research Grant from the Research Grants Council of Hong Kong and a Grant from the Hong Kong Industry Department.

Z. Jin was with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong. He is now with the Optoelectronic Laboratory, Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China.

H. S. Kwok and M. Wong are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong.

Publisher Item Identifier S 0741-3106(99)02494-5.

II. EXPERIMENTAL

Following the growth of 500 nm of thermal oxide on the starting silicon wafers, 100 nm of low-pressure chemical vapor deposited (LPCVD) a-Si was formed at 550 °C using SiH_4 as the source gas. For some of the wafers, this layer was patterned to form a more conductive source and drain "pad" regions before a second 30-nm channel layer of a-Si was deposited. Following channel layer definition, gate dielectric consisting of 100 nm of LPCVD low-temperature oxide (LTO) was deposited at 425 °C. This was immediately followed by the deposition and patterning of 300 nm of a-Si as the gate electrode. Phosphorus ions at a dose of $4 \times 10^{15}/{\rm cm}^2$ and an energy of 130 keV were implanted to dope the gate and through the LTO to form the self-aligned source and drain regions. After the implantation, any LTO not covered by the gate electrode was removed in buffered HF solution and 5 nm of Ni was blanket deposited in a high vacuum electron-beam evaporator. The wafers were heat-treated at 500 °C in an N_2 ambient for 2 h to laterally crystallize the 5-μm long channels and the implanted dopants were simultaneously activated during metal induced crystallization (MIC) of the source and drain regions. All unreacted Ni was subsequently removed in a 40% HCl solution at 60 °C. Contact holes were opened in buffered HF solution after the deposition of 500 nm of LTO as the insulation layer. The devices were sintered for 30 min in Forming gas at 450 °C after 1 μm of Al-1%Si was sputter deposited and patterned. Besides the sintering in Forming gas, no other hydrogenation process was performed. This allowed the "intrinsic" behavior of the devices to be compared and studied. A schematic structure of a TFT with an ultrathin 30-nm channel layer is shown in Fig. 1.

III. RESULTS AND DISCUSSION

Typical I_d–V_g curves of N-type TFT's with 30- and 100-nm thick channel layers are shown in Fig. 2. The channel width (W) the length (L) of the TFT's are 10 and 5 μm, respectively. Compared to the 100 nm devices, lower minimum leakage current $(I_{\rm off})$ and higher drive current $(I_{\rm on})$ were measured on the 30 nm devices—thus resulting in about 100 times increase

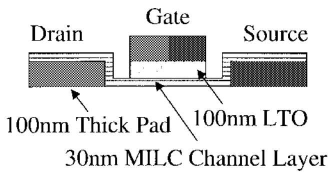

Fig. 1. Schematic cross section of an MILC TFT with 30-nm thick channel layer.

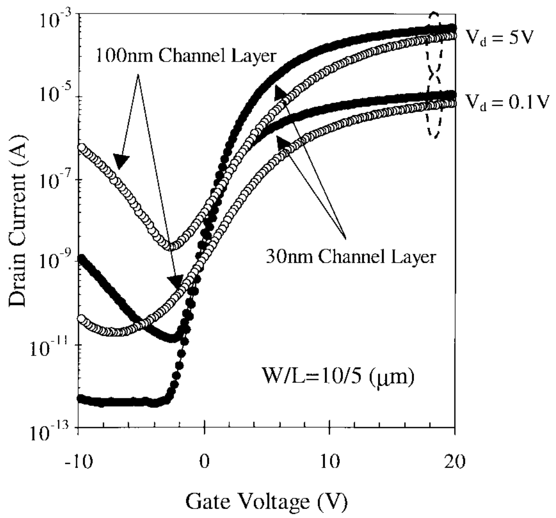

Fig. 2. I_d–V_g curves of the MILC TFT's with 30-nm (solid line) and 100-nm (dotted line) thick channel layers.

in the $I_{\rm on}/I_{\rm off}$ ratio. While it is true that the lower leakage current resulted in part from the smaller junction area in the 30-nm devices, this alone cannot account for a 50× reduction in $I_{\rm off}$. A more important reason is the better gate control of the potential through the reduced thickness of the 30-nm channel layer, which is also responsible for the correspondingly higher drive current.

A peak linear trans-conductance (g_m) of 0.076 μS was extracted for the 30-nm device, which is larger than the 0.055 μS for the 100-nm device. Assuming the validity of the following equation for the MILC TFT's:

$$g_m = \mu_{\rm FE} C_{\rm ox} \frac{W}{L} V_d$$

where $C_{\rm ox}$ is the gate capacitance per unit area, one can estimate a maximum $\mu_{\rm FE}$ of 110 cm^2/Vs for the 30-nm device. This is about 38% higher than the 80 cm^2/Vs estimated for the 100-nm device. This improvement in $\mu_{\rm FE}$ directly results from the reduced average vertical field in the ultrathin channel layers [1].

Typical I_d–V_d curves of the TFT's with 30 nm and the 100-nm thick channel layers are shown in Fig. 3. At any given V_g, the 30-nm devices exhibit higher $I_{\rm on}$ because of their higher $\mu_{\rm FE}$ and lower threshold voltage (V_T). No observable parasitic source/drain resistance induced current pinching at low V_d has been observed in the 30-nm devices. Interestingly, while the family of I_d curves for the 100-nm device shows almost ideal I_d saturation behavior, that of the 30-nm device shows a tendency of a soft breakdown at $V_d = 14$ V. Similar phenomena have been observed in SOI devices [9], in which higher drain field occurs in devices with thinner channel layers.

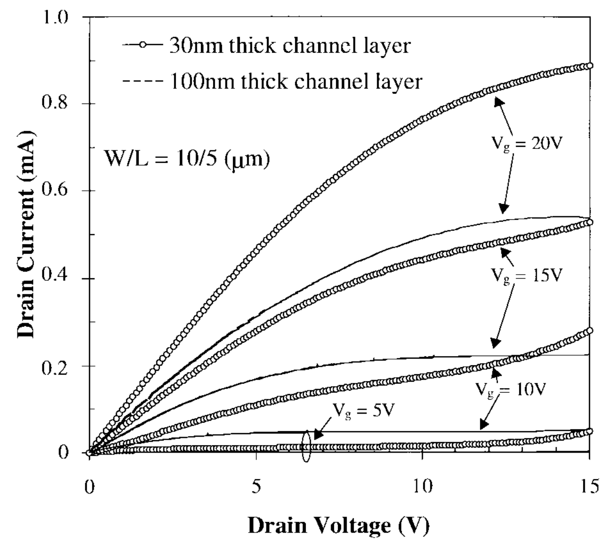

Fig. 3. I_d–V_d curves of the MILC TFT's with 30- and 100-nm thick channel layers.

TABLE I
COMPARISON OF THE PERFORMANCE OF THE DEVICES FABRICATED IN THIS WORK AND THAT OF THE DEVICES REPORTED [10]

	Devices in this work (W/L=10/5μm, MIC Gate)		Devices reported in Ref. [10] (W/L=10/10μm, Molybdenum Gate)	
	30nm thick channel layer	100nm thick channel layer	100nm thick channel layer	Novel off-set structure
μ_{FE} (cm^2/Vs)	110	80	50	50
V_T (V)	2.2	5.1	3.6 *	7 *
S (V/decade)	0.66	2.1	1.25 *	0.75 *
I_{off} (pA/μm) @ V_d = 0.1V	0.04	2	0.8 *	0.1 *
I_{on}/I_{off} ratio @ V_d = 0.1V	3x10^7	3.5x10^5	1.2x10^5 *	1x10^6 *

- Estimated from the reported I_d-V_g curves.

In Table I, the performance of the TFT's fabricated in this work and that of the MILC TFT's reported in [10] are compared. The V_T is defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L) \times 10^{-7}$ A at $V_d = 0.1$ V. The $I_{\rm on}/I_{\rm off}$ ratio is that of I_d at $V_g = 20$ V and the minimum I_d at $V_d = 5$ V.

It was proposed [11] that the high $I_{\rm off}$ in MILC TFT's resulted from an overlap of a continuous and highly defective MILC/MIC interface [8] with the drain metallurgical junction. Using an off-set structure to separate the MILC/MIC interface from the metallurgical junction, Ihn *et al.* [10] achieved significant reduction in $I_{\rm off}$. The low $I_{\rm off}$ measured on the 30-nm devices indicates that the use of thin channel layers could provide an alternative approach to $I_{\rm off}$ reduction. If the off-set structure were combined with the thin channel layers, further decrease in $I_{\rm off}$ and a corresponding increase in the $I_{\rm on}/I_{\rm off}$ ratio would be expected.

IV. SUMMARY

High performance TFT's with 30- and 100-nm thick channel layers have been successfully fabricated using nickel induced crystallization of a-Si. The highest temperature used was 550 °C for the a-Si deposition. If alternative low temperature techniques of a-Si formation were employed, such as replacing SiH_4 with Si_2H_6 [10] or using plasma activation, this would have been a 500 °C process—limited only by the MILC temperature.

Compared with the TFT's with 100-nm thick channel layers, the TFT's with 30-nm channel layers show an improvement of over 40% in $\mu_{\rm FE}$. The devices exhibit not only lower $I_{\rm off}$ but also higher $I_{\rm on}$, resulting in an increase of 100 times in the $I_{\rm on}/I_{\rm off}$ ratio. The threshold voltage and the subthreshold slope are also significantly improved. Possible reasons of the improvements have been discussed.

REFERENCES

[1] Y. Yoshimi, T. Wada, K. Kato, and H. Tango, "High performance SOI MOSFET using ultra-thin SOI film," in *IEDM Tech. Dig.*, 1987, p. 640.

[2] J. P. Colinge, "Reduction of floating substrate effects in thin-film SOI MOSFET's," *Electron. Lett.*, vol. 22, no. 4, p. 187, 1986.

[3] J. C. Sturm, K. Tokunaga, and J. P. Colinge, "Increased drain saturation current in ultra-thin silicon-on-insulator (SOI) MOS transistors," *IEEE Electron Device Lett.*, vol. 9, p. 460, Sept. 1988.

[4] M. Miyasaka, T. Komatsu, W. Itoh, A. Yamaguchi, and H. Ohshima, "Effects of semiconductor thickness on poly-crystalline silicon thin film transistors," *Jpn. J. Appl. Phys.*, vol. 35, p. 923, 1996.

[5] T. W. Little, K. I. Takahara, H. Koike, T. Nakazawa, I. Yudasaka, and H. Ohshima, "Low temperature poly-Si TFT's using solid phase crystallization of very thin films and an electron cyclotron resonance chemical vapor deposition gate insulator," *Jpn. J. Appl. Phys.*, vol. 30, no. 12B, p. 3724, 1991.

[6] H. Kuriyama, S. Kiyama, S. Naguchi, T. Kuwahara, S. Ishida, T. Nahda, K. Sano, K. Iwata, S. Tsuda, and S. Nakano, "High mobility poly-Si TFT by a new Excimer laser annealing method for large area electronics," in *IEDM Tech. Dig.*, 1991, p. 563.

[7] S. W. Lee and S. K Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, pp. 160–162, Apr. 1996.

[8] J. H. Jin, G. A. Gururaj, M. Yeung, H. S. Kwok, and M. Wong, "Nickel induced crystallization of amorphous silicon thin films," *J. Appl. Phys.*, vol. 84, no. 1, pp. 194–200, July 1998.

[9] M. Yoshimi, M. Takahashi, T. Wada, K. Kato, S. Kambayashi, M. Kemmochi, and K. Natori, "Analysis of the drain breakdown mechanism in ultra-thin-film SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 37, p. 2015, Sept. 1990.

[10] T. H. Ihn, B. I. Lee, T. K. Kim, K. H. Kim, J. W. Shin, P. S Ahn, W. C. Jeong, and S. K. Joo, "Fabrication of metal-gate poly-Si TFT's by metal induced lateral crystallization," in *SID Dig.*, 1997, p. 188.

[11] G. A. Bhat, Z. H. Jin, H. S. Kwok, and M. Wong, "The eEffects of the MILC/MIC interface on the performance of MILC-TFT's," in *Dig. 56th Device Research Conf.*, June 1998, pp. 110–111.