Experimental Characterization of P-channel Polysilicon Conductivity Modulated Thin-Film Transistors

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Abstract

A p-channel poly-Si CMTFT (Conductivity Modulated Thin-Film Transistor) is demonstrated and experimentally characterized. The transistor uses the concept of conductivity modulation in the offset region to obtain a significant reduction in on-state resistance. This structure can provide 1.5 to 2 orders of magnitude higher on-state current than that of the conventional offset drain TFT at drain voltage ranging from -15V to -5V while still maintaining low leakage current and simplicity in device operation. The p-channel CMTFT can be combined with the n-channel CMTFT to form CMOS high voltage drivers, which is very suitable for use in fully integrated large area electronic applications.

key words polysilicon, conductivity modulated thin-film transistor, high voltage driver

Introduction

Low temperature polysilicon TFT (thin-film transistor) appears to be one of the most promising technologies for the ultimate goal of building large area electronic systems on glass substrate [1]. In flat panel liquid crystal, electroluminescent, and plasma displays as well as other applications such as high speed printers and page width optical scanners, etc., both efficient high voltage drivers and control circuits have to be implemented on the same glass substrate for system integration [2]. For high voltage drivers, conventional offset drain TFT is commonly used [3]. This structure has severe current pinching problem, which results in very high on-state resistance. The low concentration offset implant and field plated offset approaches were proposed [4][5]. However, both of these approaches are very difficult to be implemented. Recently, an n-channel conductivity modulated TFT (CMTFT) was proposed to solve the current pinching problem [6]. The device uses the concept of conductivity modulation in the offset region. Experimental results showed that it can provide orders of magnitude higher on-state current compared to the conventional offset drain TFT while still maintaining low leakage current. To further minimize the power dissipation and to facilitate circuit design, CMOS high voltage drivers should be used. Thus, a high performance p-channel CMTFT is needed.

In this paper, a p-channel poly-Si CMTFT is demonstrated and experimentally characterized. Results show that conductivity modulation in the p-channel CMTFT device is as effective as that in the n-channel device. Fabrication process, on-state/off-state I-V characteristics, and breakdown voltage performance of the p-channel CMTFT will also be discussed.

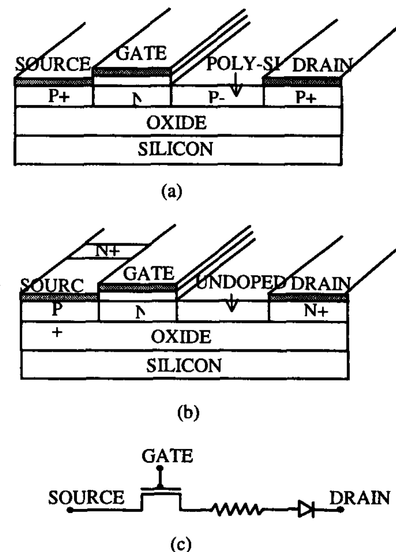

Fig. 1. Schematic cross-section of (a) the p-channel conventional offset drain TFT, (b) the CMTFT, and (c) the equivalent circuit of the p-channel CMTFT.

Device Structure and Fabrication

Schematic cross-section of the p-channel conventional offset drain TFT and CMTFT are shown in Fig. 1 (a) and (b). Channel region of the devices is lightly doped to n-type to make sure the device can be operated in the inversion mode with low leakage current and adjustable threshold voltage. For the CMTFT, the drain and offset regions can be viewed as a series combination of a diode with a drift resistance as shown in Fig.1(c). In order to prevent minority carrier (electron) accumulation in the channel region, it is necessary to connect the channel region of the device to the source. A segmented source structure with 10:1 segmentation ratio (p^+ to n^+) is used as shown in Fig. 1 (b).

To demonstrate the performance of the p-channel CMTFT, both the p-channel conventional offset drain TFT and CMTFT have been fabricated on the same substrate using low temperature (600°C) process. The major fabrication steps of the p-channel CMTFT are

shown in Fig. 2. Silicon wafers with a layer of thermally grown oxide (5000Å) are used as starting substrate. A layer of a-silicon (2000Å) is first deposited on the oxide at 550°C using LPCVD. It is then recrystallized to polysilicon by furnace annealing at 600°C in N_2 ambient for 20 hours. After the device islands are defined, channel region of the devices is then doped with phosphorus. In the case of the conventional offset drain TFT, boron implant with dose of $1x10^{12}$ cm^{-2} is used to dope the offset region. After that, a layer of gate oxide (1000Å) is deposited using APCVD. The gate polysilicon is then deposited at 600°C using LPCVD with a thickness of 2500Å After that, it is doped by phosphorus implant and patterned. The source region is doped by boron implant, and the drain region is doped by phosphorus. After the source/drain implantation, 3500Å of LTO is deposited and densified at 600°C in oxygen ambient for 10 hours and in nitrogen ambient for 2 hours. The dopants are activated during the LTO densification. Contact holes on the LTO layer are opened using dry etching. After metal deposition and patterning, forming gas annealing is performed at 400°C for 30 minutes. Finally, the devices are hydrogenated in r.f. hydrogen plasma for 2 hours.

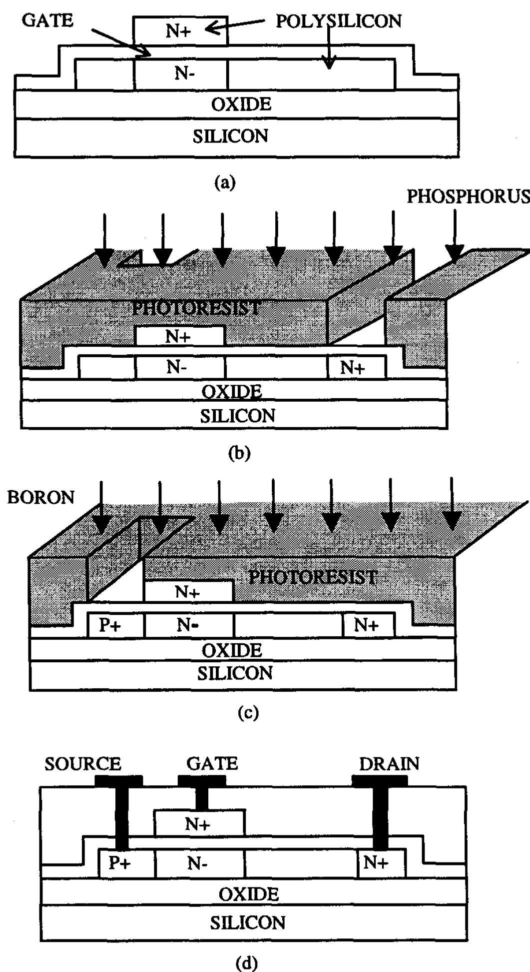

Fig. 2. Major fabrication steps of the p-channel CMTFT.

Results and Discussion

Fig. 3 shows the forward conduction characteristics of the conventional offset drain TFT and CMTFT. Both devices have the same offset length of 3μm and W/L ratio of 200 μm/5 μm. It is shown that the conventional offset drain TFT experiences severe current pinching due to the high resistance in the lightly doped offset region. In the case of the CMTFT, also shown in Fig. 3, the current pinching problem is minimized. This is the

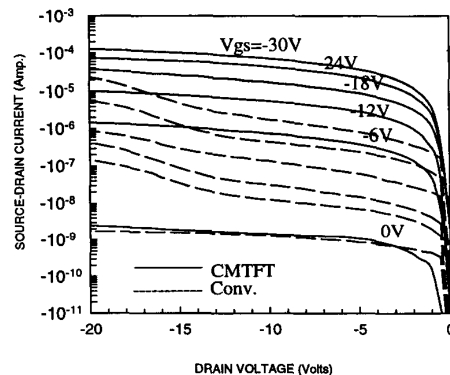

Fig. 3. Forward conduction characteristics of the p-channel CMTFT and conventional offset drain TFT.

result of the electrons injected from the drain, which modulates the offset region and reduces the on-state resistance significantly. From Fig. 3, the on-state current of the CMTFT is 1.5 to 2 orders of magnitude higher than that of the conventional offset drain TFT at a gate voltage of -24V and drain voltages ranging from -15V to -5V.

Fig. 4 shows the gate transfer characteristics of the p-channel conventional offset drain TFT and CMTFT before and after hydrogenation. Both devices have the same dimensions as those stated in Fig. 3. The threshold voltage, subthreshold slope, and leakage current are all improved after hydrogenation for both devices. The leakage current of the CMTFT is comparable with that of the conventional offset drain TFT. At a drain voltage and gate voltage of -20V and -24V, the on/off current ratio of the CMTFT is six times larger than that of the conventional offset drain TFT.

The on-current and off-current of the CMTFT as a function of offset length are shown in Fig. 5 with a W/L ratio of 200 μm/5 μm. The on-current is measured at a drain bias of -20V and a gate bias of -24V. As expected, the on-current of the CMTFT decreases with the increase in offset length. This is due to the increase in the on-state resistance of the device with longer offset length. The off-current is measured at a drain bias of -20V and a gate bias of 0V. The off-current also decreases with the increase in offset length. This is due to the reduction of the lateral electric field at the drain. A relatively constant on/off current ratio is obtained and also shown in Fig. 5.

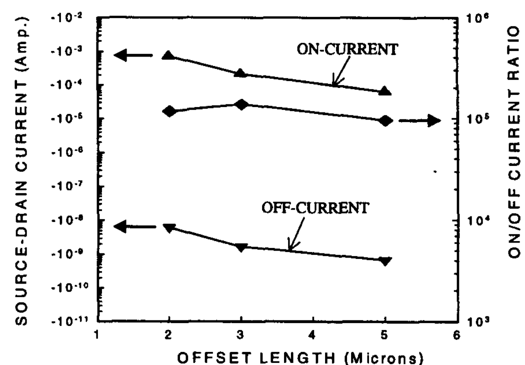

Fig. 5. On- and off-current vs. offset length.

Fig. 6 shows typical forward blocking characteristics of the p-channel CMTFT and conventional offset drain TFT (V_{gs}=0V). The breakdown voltages (defined at a drain current of -100nA/μm channel width) of the CMTFT and conventional offset drain TFT are -46V

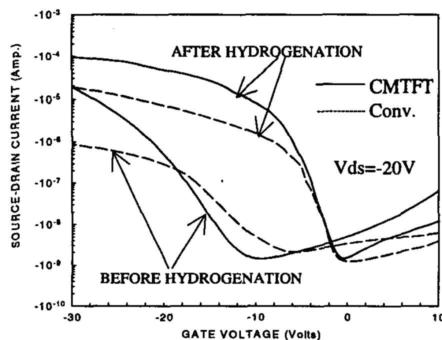

Fig. 4. Transfer characteristics of the p-channel CMTFT and conventional offset drain TFT.

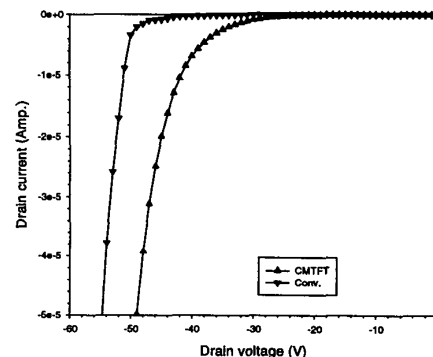

Fig. 6. Blocking characteristics of the p-channel CMTFT and conventional offset drain TFT.

and -53V, respectively. In the forward blocking regime, the CMTFT behaves like a nonlinear resistor represented by the n^+ (segmented) /n^- /i/n^+ parasitic resistor. In the case of the conventional offset drain TFT, the breakdown voltage can be considered as the BV_{CEO} of the $p^+/n^-/p^-/p^+$ parasitic bipolar structure.

Although the p-channel CMTFT has involved minority carriers (electrons) in the conduction mechanism, there is no degradation observed in the switching speed of the device compared to that of the conventional offset drain TFT. This is the result of the very short lifetime of the minority carriers (electrons) in polysilicon film.

Conclusions

A p-channel poly-Si CMTFT is demonstrated and experimentally characterized. Results showed that the concept of conductivity modulation in the p-channel device is as effective as that in the n-channel device. With the increase in offset length, higher breakdown CMTFT driver devices can be obtained. The p-channel CMTFT, together with the n-channel counterpart, can be used to implement CMOS high voltage drivers for a variety of fully integrated large area electronic applications which require high voltage driving capability.

References

[1] K. Werner, "The flowering of flat displays," *IEEE Spectrum*, pp.40-49, May 1997.

[2] M. G. Clark, "Current status and future prospects of poly-Si devices," *IEE Proc. Circuits Devices Syst.*, Vol. 141, No.1, pp.3-8, 1994.

[3] M. Hack, A. Chiang, T. Y. Huang, A. G. Lewis, R. A. Martin, H. Tusan, I. W. Wu, and P. Yap, "High voltage thin-film transistors for large area electronics," *IEDM Tech. Dig.*, pp.252-255, 1988.

[4] K. Tanaka, H.Arai, and S. Kohda, "Characteristics of offset-structure polycrystalline silicon thin-film transistors," *IEEE Electron Device Lett.*, Vol.9, No.1, pp.23-25, 1988.

[5] T. Y. Huang, I-Wei Wu, A. G. Lewis, A. Chiang, and R. H. Bruce, "A simpler 100V polysilicon TFT with improved turn-on characteristics," *IEEE Electron Device Lett.*, Vol.11, No.6, pp.244-246, 1990.

[6] Anish Kumar K. P., Johnny K. O. Sin, Man Wong, and Vincent M. C. Poon, "A conductivity modulated thin-film transistor," *IEEE Electron Device Lett.*, Vol.16, No.11, pp.521-523, 1995.