The Effects of MIC/MILC Interface on the Performance of MILC-TFTs

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High mobility, low temperature poly-crystalline silicon thin film transistors (poly-Si TFT) potentially enables the integration of driver circuits and pixel transistors on the same glass panel for large area displays. Solid phase crystallized TFTs (SPC-TFT) have been studied extensively at processing temperature of about 600°C. However, due to the presence of the large density of intra- and inter-granular traps, SPC-TFTs suffer from poor device performance, such as high threshold voltage (V_T), high leakage current (I_{off}) and early kink effect (V_k). Metal induced lateral crystallization (MILC) [1] at 500°C is an alternative technology for re-alizing TFTs. Due to the presence of large longitudinal grains and lower trap densities [2], these devices exhibit better performance than SPC-TFTs. With self-aligned deposition of the crystallization inducing metal, it is discovered that the behavior of conventional MILC-TFTs is strongly influenced by the overlapping of the drain metallurgical junction and the MIC/MILC interface, which consists of a grain boundary and trapped metallic impurities. Detrimental effects of this overlap can be eliminated by separating the interface from the junction. In this work, the performance of SPC- and MILC-TFTs are compared, particularly with regard to scalability and the onset of the kink effect.

TFTs without (cMILC-TFTs) and with (oMILC-TFTs) a deliberate offset between the edges of the crystallization inducing metal and the gate were fabricated at 500°C. Schematic structures of these devices are shown in Figure 1. For comparison, TFTs were also constructed using SPC at 625°C. The variations of V_T and I_{off} with channel length (L) are plotted in Figures 2 and 3, respectively. It is clear that V_T roll-off occurs at a longer channel length for SPC-TFTs, thus making them less scalable than MILC-TFTs. On the other hand, while the I_{off} for SPC-TFTs is only weakly dependent on L, that for MILC-TFTs is highly sensitive to reduction in L, especially for short channel devices. We proposed that the better scalability of MILC-TFTs was a result of the growth of grains longitudinal to the direction of current flow, whereas the high sensitivity of I_{off} was related to the overlap of the highly defective MIC/MILC interface and the drain metallurgical junction.

Substrate current (I_{sub}) resulting from a sufficiently large drain voltage (V_d) is known to lower V_T via a modulated body potential. This is manifested as current kinks in the I_d-V_d curves. Due to the better material quality in MILC poly-Si, one would expect less severe kink effect in MILC-TFTs than in SPC-TFTs. In Figure 4, I_d normalized by the drain current at the kink (I_k) is plotted against V_d. It is clear that for any given L, the V_k is lower in cMILC- than in SPC-TFTs. The implied higher I_{sub} again results from the much increased trap-assisted field emission current resulting from the overlap of the defective MIC/MILC interface and the drain metallurgical junction in cMILC-TFTs. In oMILC-TFTs, I_{sub} can be significantly reduced and the onset of the kink effect can be delayed by the offset that separates the defective MIC/MILC interface from the high electric field within the depletion region of the junction. This improvement is shown in Figure 5. It is expected, and indeed has been demonstrated [3], that I_{off} is lower in oMILC- than in cMILC-TFTs.

References

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3. T. H. Ihn, B. I. Lee, T. K. Kim, K. H. Kim, J. W. Shin, P. S. Ahn, W. C. Jeong and S. K. Joo, "Fabrication of Metal-gate poly-Si TFTs by Metal Induced Lateral Crystallization", Digest of Technical Papers, SID 1997, p188-191.

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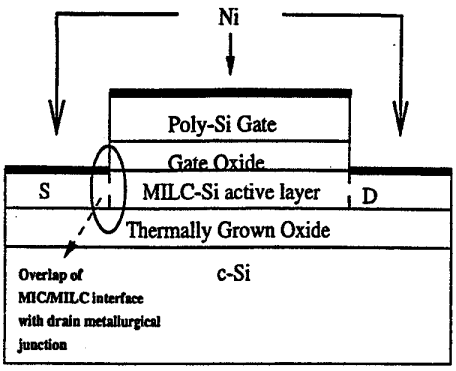
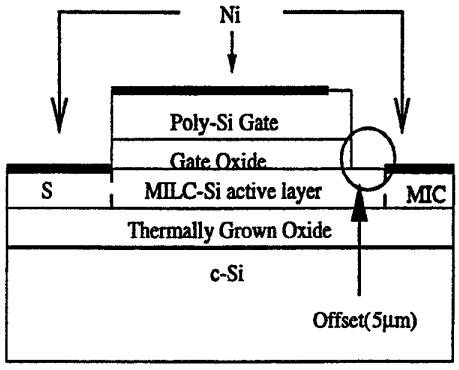


a)



b)

Figure 1. Schematic diagram of MILC-TFTs a) without b) with the Ni offset. Poly-Si active layer and gate oxide thickness is 100nm each.

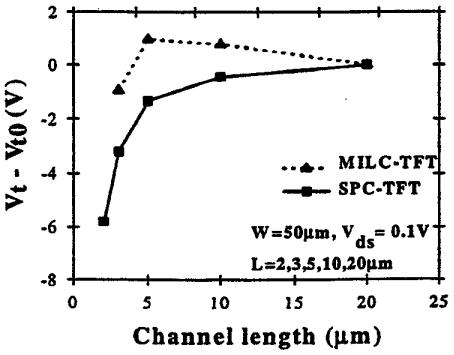


Figure 2. Dependence of V_t on L for cMILC-TFT and SPC-TFT. V_{to} is the threshold voltage of the device with the longest channel length.

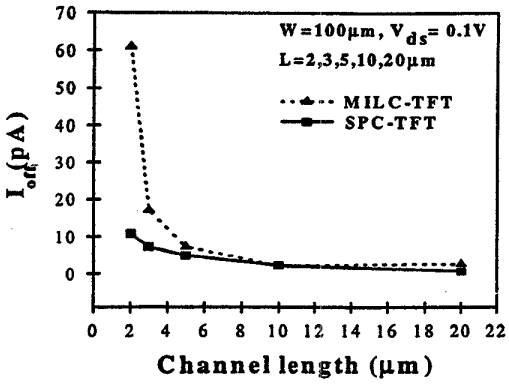


Figure 3. Sensitivity of off-state current (I_{off}) on channel length.

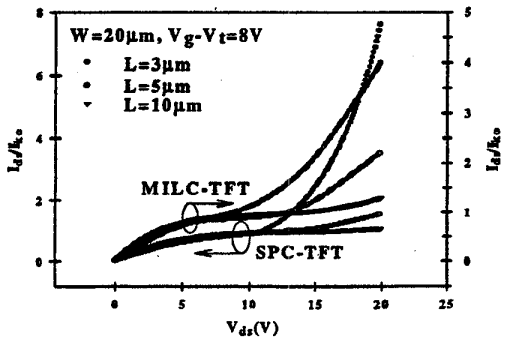


Figure 4. Normalized output current characteristics of cMILC- and SPC-TFTs at common gate drive. 'I_{ko}' is the drain current at the onset of kink effect.

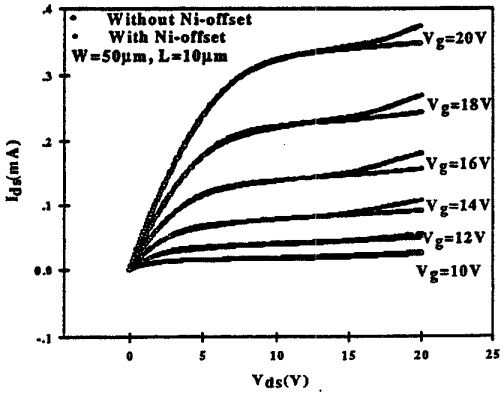


Figure 5. Output characteristics of cMILC- and oMILC-TFTs.