INTEGRATED DIGITAL INPUT DRIVER FOR ACTIVE MATRIX LIQUID-CRYSTAL-ON-SILICON DISPLAY

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Abstract

A digital input driver was designed and integrated with an active matrix nematic liquid-crystal-on-silicon (LCOS) display. Fabricated by conventional 2-μm CMOS technology, the driver in the periphery of the active matrix can easily incorporate versatile electronic functions into the silicon backplane. This integration makes the LCOS display easier to be interfaced with different image sources of various formats and, hence, leads to a versatile display system.

INTRODUCTION

Crystalline silicon has been used as an alternative approach for the fabrication of active matrix liquid crystal display (AMLCD)[1-4]. The advantages are the better electronic properties of crystalline silicon material and the more matured VLSI technology. Very sophisticated driver circuitry can be easily integrated into periphery of the display. The driver circuitry is to download image data to the active matrix and render the image on the display. The monolithic integration of driver into the display also helps simplify the interconnection and packaging problems of the display system.

In general, the LCOS display was integrated with analog input driver to render grey-level images[1]. This type of display, usually filled with nematic liquid crystal, can accept directly CRT-compatible analog signals. Another technique was to utilize time-multiplexing frames with binary input driver to drive ferroelectric liquid crystal for grey-level representation[2]. In our work, the display was integrated with a 3-bit digital input driver. We believe that the digital input scheme can provide more accurate voltages in much higher speed to the display for a more versatile display system. The expense is at the circuit complexity and real estate of wafer.

SILICON BACKPLANE

The silicon backplane of the LCOS display consists of a data driver on the top, a scan driver on the side and an active matrix in the center as shown in Figure 1. The three digital data inputs are loaded in serial into the input shift registers and transferred in parallel to the level-shifting latches when a full line of data are loaded. These latched data further select among eight reference voltages through analog multiplexers to drive one row of display selected by the scan driver. The driving voltage of these latched data is also pulled up from 5V to 12V to allow for higher pixel voltage to be transferred.

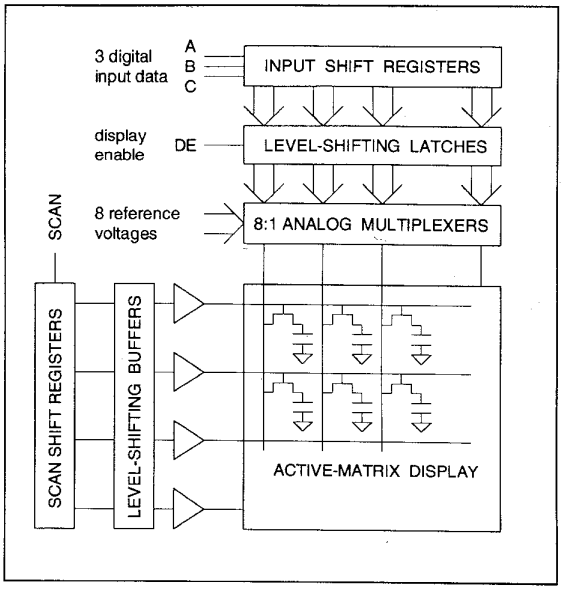

Figure 1. Digital input drivers integrated with the active matrix display.

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The scan driver consists of shift registers to shift in scan pattern and level-shifting buffers to activate scan lines. Whereas, the scan line voltage is also pulled up to allow for higher pixel voltage to be transferred.

The central area is the two-dimensional array of dynamic storage cells which consists of a single NMOS transistor and a storage capacitor. With 2-metal and 1-poly structure, the pixel area is well covered by either metal or polysilicon layers. Whereas, metal-1 layer forms the vertical bit line, polysilicon forms the horizontal word line, and metal-2 layer acts as the mirror reflector on the top of pixel. The pixel pitch is 50μm and the aperture ratio is 85%. With 2-μm design rules, the NMOS transistor occupies less than 500μm^2, or 20% of the pixel area. The remaining area gives rise to a storage capacitance of 780fF. This storage capacitor is inserted into the pixel structure to hold the charge. The large capacitor area also helps improve the planarization of pixels.

The silicon backplane was fabricated with a projection aligner as the photolithography tool. Figure 2 shows photograph of one corner of the silicon backplane. Both the data driver on the top and scan driver on the right are visible together with the active matrix.

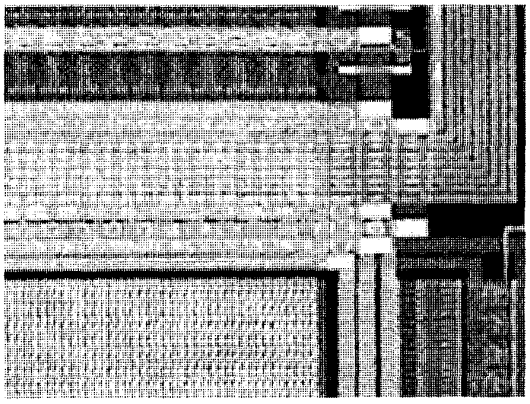


Figure 2. Photograph of the silicon backplane.

LIQUID CRYSTAL CELL

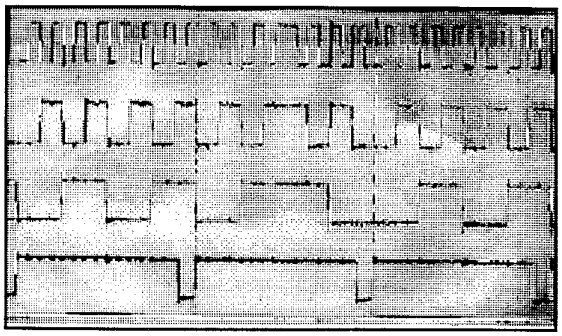
The silicon backplane, after wafer-level probing for the integrity of drivers, was ready for liquid crystal cell fabrication. To yield grey-level control of the images, nematic liquid crystal with smooth transmission-voltage characteristic was chosen.

The fabrication of LCOS cell concerns filling a thin layer of liquid crystal between the silicon backplane and a flat cover glass on the top. The cover glass is coated with an indium tin oxide transparent electrode and then a thin layer of polyimide for alignment. The cell gap between the silicon backplane and glass plate is controlled by even distribution of spacer to yield the required retardation. The assembly is conducted in vacuum and the cell is filled by capillary force with the liquid crystal mixture.

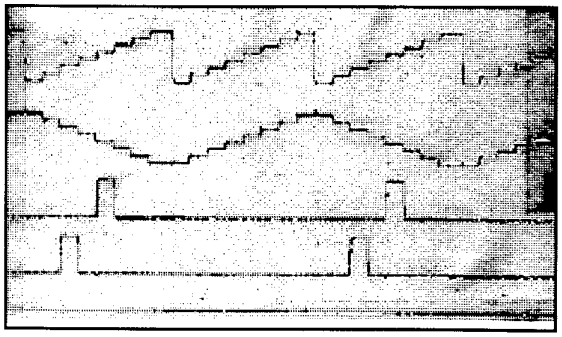
ELECTRICAL CHARACTERIZATION

After wire bonding of the LCOS cell onto a printed circuit board, the electronic properties of the peripheral driver circuitry were then firstly characterized. This involves mainly the verification of driver functions, sampling of pixel voltage at different locations and measurement of transients. The electronic characterization was conducted with an IMS tester to generate test patterns and a digitizing oscilloscope for transient measurements. It was found that the driver can run at a data clock up to 30MHz without faults. Beyond 30MHz, the drivers might occasionally lost synchronization due to very long clock and control signal lines across the chip. With the digitizing oscilloscope, it was also found that the deviation of pixel voltage was less than 10mV across the whole active matrix of 0.8 inch diagonal.

Figure 3 shows the system timing diagram of a smaller test display of 16 by 16 pixels. As shown in Figure 3(a), three digital data inputs A, B and C are shifted into the display, followed by a display enable signal DE to trigger the transfer of data in parallel to the latches when a full line of data is loaded. As shown in Figure 3(b) are eight grey-level voltages in ascending and descending orders of two different bit lines, as well as two word line signals.



(a)



(b)

Figure 3. System timing diagram of the driver: (a) 3 digital data inputs A, B, C and display enable signal DE; (b) driving voltages of two column and two scan-line signals. Data clock is 10MHz.

OPTICAL CHARACTERIZATION

To characterize optical properties of the LCOS cell, we have arranged an optical setup which consists of a collimated light source, a polarizing beam splitter, a power meter and lens system. Test patterns were again generated by the IMS tester and sent to the cell at various refresh rates and frame rates. It was found that the photocurrent induced by light illumination on the cell could still discharge the pixel voltage, though each pixel was well shielded by either metal or polysilicon layers. This cause a reduction in contrast ratio through the whole display panel. The contrast ratio can be greatly improved by increasing the refresh rate per frame. By varying the refresh rate and monitoring the contrast ratio, the decay time of pixel voltage was estimated to be around 1.2 ms.

While the increase of refresh rate can help maintain the pixel voltage and hence improve the contrast ratio, different frame rates can affect the optical performance of liquid crystal and hence the contrast ratio, too. By varying the frame rate while maintaining the refresh rate, we were able to determine a best frame rate at which the contrast ratio was optimized. It was found that this best frame rate was 200Hz, a figure concurred by the rise time and falling time of liquid crystal which were 2 and 4 ms, respectively.

A PROTOTYPING DISPLAY SYSTEM

With these characterization data, we were able to design an interface controller to interpret different kinds of image data and write to the LCOS cell. Figure 4 shows a block diagram of the interface controller used with the LCOS cell. The major components of this interface controller are a phase-locked loop (PLL) pixel clock generator to retrieve the data clock, a cache memory to store image data, and application specific integrated circuits (ASICs) to perform logic control and reformat data for the LCOS cell.

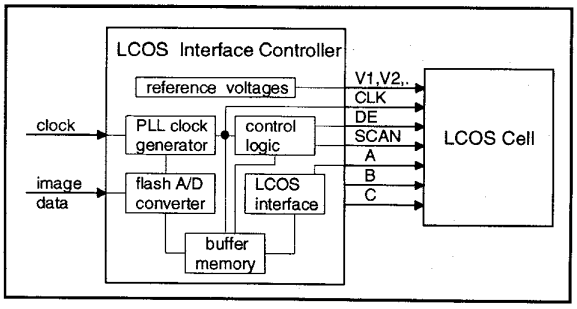


Figure 4. Block diagram of the interface controller along with the LCOS cell.

Figure 5 shows a HKUST logo at one corner of the LCOS cell and projected by a 50X zoom lens onto a screen. The pattern was sent to the cell at a clock rate of 25MHz, a frame rate of 200Hz and a refresh rate of 800Hz, or 4 refreshes per frame. Frame inversion technique and AC driving scheme were adopted for this prototyping projection display system.

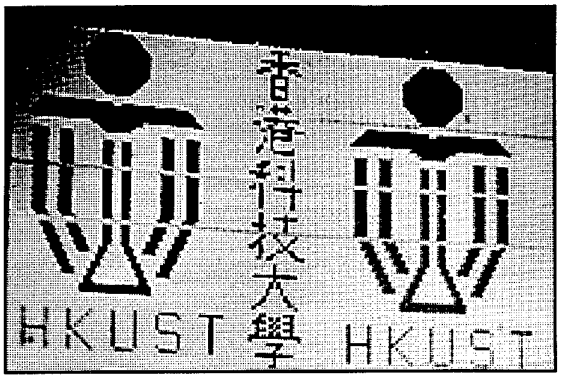


Figure 5. Photograph of a HKUST logo projected by the prototyping display onto a screen.

CONCLUSION

We have developed a nematic liquid-crystal-on-silicon display with integrated digital input driver. The advantages of using digital input scheme for the display is the better control of pixel voltages and higher speed of data rate. A data clock up to 30MHz and a pixel voltage deviation less than 10mV across the display of 0.8 inch diagonal has been demonstrated. With digital input scheme, each reference voltage can be tailored to yield most equalized grey scale for particular liquid crystal and display application. In addition, digital input scheme also makes the display system easier to interface with different image data of various format. The major disadvantages are at the expense of circuit complexity and expensive real estate of wafer. The generally small size of LCOS cell and associated bulky optics for polarization control may prevent its applications from transmissive and direct-viewing display. But utilizing the VLSI technology for better driver design and functions, LCOS cell may see applications in spatial light modulation and high information content projection-type display.

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REFERENCES

[1] J. P. Salerno, "Single Crystal Silicon AMLCDs", Proc. IDRC'94, pp.39-44, 1994.

[2] K. Johnson, D. Mcknight and I. Underwood, "Smart Spatial Light Modulators Using Liquid Crystals On Silicon", IEEE Journal of Quantum Electronics, Vol. 20. No. 2, p. 699-714, 1993.

[3] P. Alvelda and T. F. Knight, Jr., "Ferroelectric Microdisplays Using Distortion-Compensated Pixel Layouts", SID 95 Digest, p.931-933, 1995.

[4] W.-D. Molzow, W. Brinker, W. Wirges, R. Gerhard-Multhaupt, R. Melcher, W. Budde and H.-L. Fiedler, "Active silicon CMOS addressing matrices for light-valve projection displays", Displays, Vol. 6, No. 1, pp.21-26, 1995.