FAST PROTOTYPING OF VIDEO INTERFACE CONTROLLER FOR AMLCD SYSTEM

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Abstract - A video interface controller for reflective silicon-based AMLCD was developed. By using field programmable gate array (FPGA) as an application specific integrated circuit (ASIC), system design flexibility and fast prototyping were achieved. This controller can display both progressive VGA and interlaced NTSC signals in various data inversion formats. The video interface controller and associated silicon based AMLCD panel can lead to a versatile multimedia display system.

I. INTRODUCTION

Crystalline silicon has been used as an alternative approach for the fabrication of active matrix liquid display (AMLCD)[1-4]. The advantages are better electronic properties of crystalline silicon material and the more matured VLSI technology. Very sophisticated driving circuitry can be easily integrated into periphery of the display. In our earlier work, a silicon-based AMLCD with integrated digital driving circuitry was developed for reflective display. The integrated digital drivers are to download the image data to the active matrix and render the image on the display. In general, the digital input scheme can provide more accurate voltage in much higher speed to the display for a more versatile display system[5].

The silicon backplane of the silicon-based active matrix crystal display (AMLCD) consists of a digital data drivers on the top, a scan drivers on the side and an active matrix in the centre as shown in figure 1. The four digital data inputs are loaded in serial into the input shift registers and transferred in parallel to the level-shifting latches when a full line of data are loaded. These latched data further select among sixteen reference voltage through the analog multiplexers to drive one row of display selected by the scan driver. Figure 2 shows the photograph of one corner of the silicon backplane. Both the data driver on the top and scan driver on the right are visible together with the active matrix.

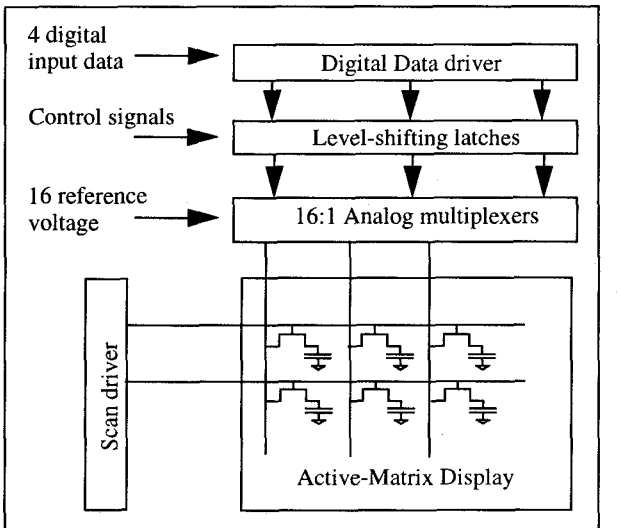

Figure 1 Digital input drivers integrated with the active matrix display

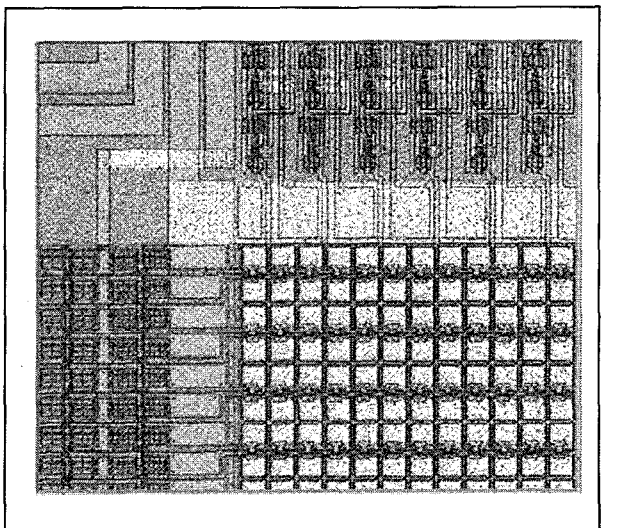

Figure 2 Photograph of the silicon backplane

In this work, a video interface controller was developed to display both progressive VGA and interlaced NTSC signals in various data inversion formats on the silicon-based AMLCD. Field programmable gate array (FPGA) was used as an application specific integrated circuit (ASIC) to achieve design flexibility and fast prototyping.

II. VIDEO INTERFACE CONTROLLER

The video interface controller can be divided into analog and digital parts. The analog part consists of pixel clock generator, video amplifiers, flash analog to digital converters and analog voltage sources. It also include a NTSC decoder to decompose composite NTSC signal to analog video. The digital parts consists of an ASIC for logic control and data flow manipulation, as well as buffer memory for data storing. The analog part is the front end of the interface controller to receive the VGA and NTSC video analog signals and converts to digital format. The synchronization signals such as Vsysc, Hsysc and dot clock are also provided by this part. The digital part is to provide all timing control signals and video data management between the AMLCD panel and controller. The digitized video data are saved into the buffer memory and then progressively sent to the AMLCD panel. Figure 3 shows the block diagram of this video interface controller.

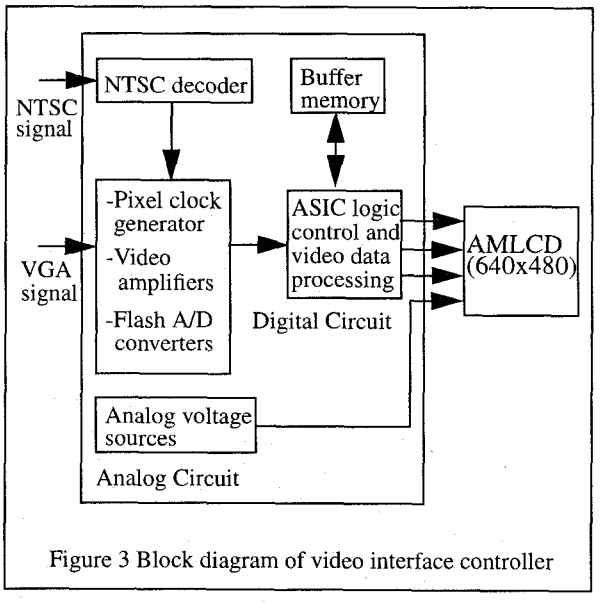

Figure 3 Block diagram of video interface controller

III. ANALOG PART

In the analog part, it contains the phase-locked loop (PLL) pixel clock generator which is used to synthesize the dot clock. In the video display, the dot clock frequency is 25MHz and 12.17MHz for progressive VGA and interlaced NTSC respectively. In general, the pixel clock generator provides the progressive VGA clock. The Hsysc signal is used of the PLL reference frequency for synchronization purpose. The VGA clock can be further divided by a certain factor when the interlaced NTSC display is required. So the same PLL pixel clock generation circuit can be used to generate the dot clock for both progressive VGA and interlaced NTSC video. On the other hand, a flash analog to digital conversion circuit is required to convert the analog video data to digital format. Up to eight bits resolution digital RGB video data can be provided by this A/D conversion circuit. Odd and even columns digital video data can be separated by using two A/D converters and two phase clocks sampling scheme. Further, the video amplifiers are used to amplify the video analog data before the analog to digital conversion in order to achieve higher data precision. In addition, the NTSC decoder is included to the analog part. It is utilized to decompose the NTSC composite video signal to the analog R, G and B and corresponding synchronization signals which are Vsysc and Hsysc signals. The block diagram of analog part is shown in figure 4.

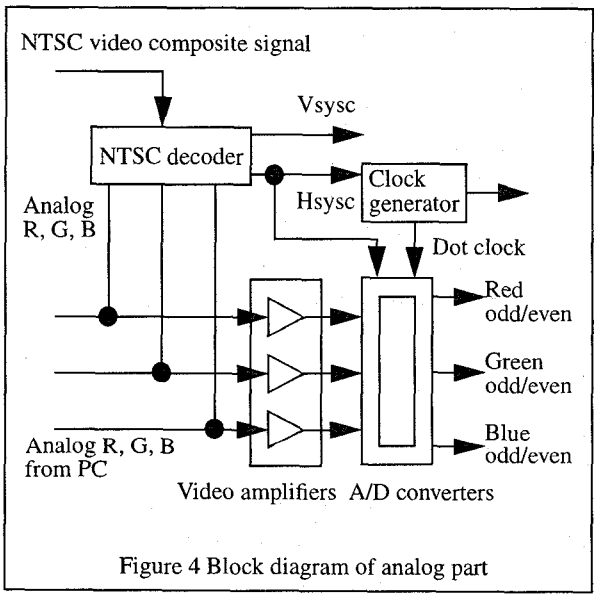

Figure 4 Block diagram of analog part

IV. DIGITAL PART

In the digital part, an application specific integrated circuit (ASIC) is the major system component. The field programmable gate array (FPGA) is used to implement the ASIC design because of its fast prototyping and flexible design characteristics. This ASIC is utilized for video data manipulation and display timing and synchronization control functions. In general, both the VGA and NTSC video have about the same resolution of 640 by 480 pixels. Therefore, an AMLCD panel of 640 by 480 pixels can be used to display either type of video. However, the display sequence for the VGA is progressive while the NTSC is interlaced. This discrepancy is resolved in the video interface controller by using a buffer memory to store a whole frame of video data in progressive order. By combining the buffer memory, the video interface controller has a capability to continuous capture both progressive and interlaced video frames and then progressively sent to the AMLCD panel without missing the video data. Furthermore, all control and timing signals which are applied to the AMLCD panel and internal logic control circuits are generated by the ASIC. These signals are according to the system timing requirements of the AMLCD system. Figure 5 shows the block diagram of digital part.

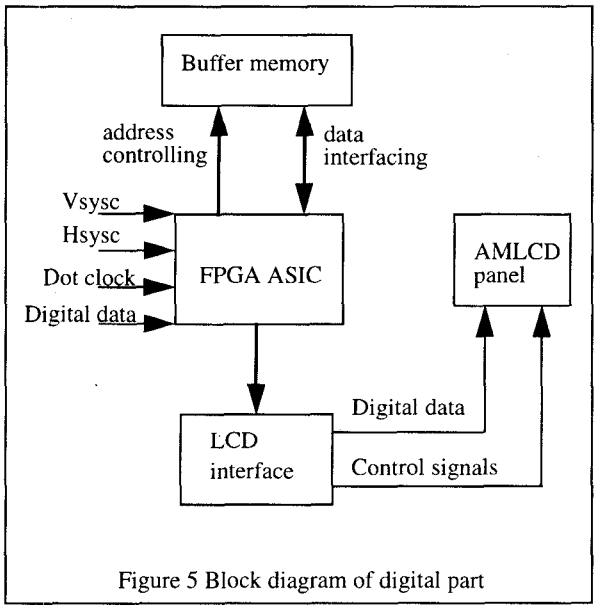

Figure 5 Block diagram of digital part

The digital circuit consists of a Xilinx XC4006 field programmable gate array for the design of ASIC, four SRAMs for data storing and the LCD interfacing circuits between the video interface controller and AMLCD panel. The capacity of the memory is determined on the display resolution and how many bits are used to represent of each pixel data. On the other hand, this ASIC can also control the output video data from the memory to the AMLCD panel with different polarity inversion schemes such as dot conversion, line conversion, column conversion and frame conversion. In addition, the refresh rate of frame data is increased from the 60Hz for both VGA and NTSC signals to 240Hz for the AMLCD panel by the ASIC with a much faster pixel clock is applied. Therefore, the frame rate control (FRC) can be achieved by changing the pixel clock frequency. For the circuit design complexity, the equivalent gate count is 4200 for progressive VGA and 4500 for interlaced NTSC. By using FPGA technology, a fast prototyping and design flexibility can be achieved. Hence, the lead time and manufacturing cost can be lower. Figure 6 shows the partial layout of VGA display using XC4006 FPGA.

V. AMLCD CHARACTERIZATION

In the experiment, the video interface controller is utilized to download either progressive VGA or interlaced NTSC to the reflective silicon-based active matrix liquid crystal display (AMLCD) panel. By using field programmable gate array as an application specific integrated circuit, we are able to tailor quickly the video interface controller for different video format. Figure 7 shows some of video images from PC and rendered on the display for projection and direct view through the polarizing lenses. From the display results, a fine images such as cursor and poker can be clearly identified.

VI. CONCLUSION

We have developed a versatile video interface controller to display and optimize the video images on the AMLCD system. This interface controller can display

both progressive VGA and interlaced NTSC video. We believe that this fast prototype video interface controller and associated reflective silicon based AMLCD panel can lead to a versatile multimedia display system.

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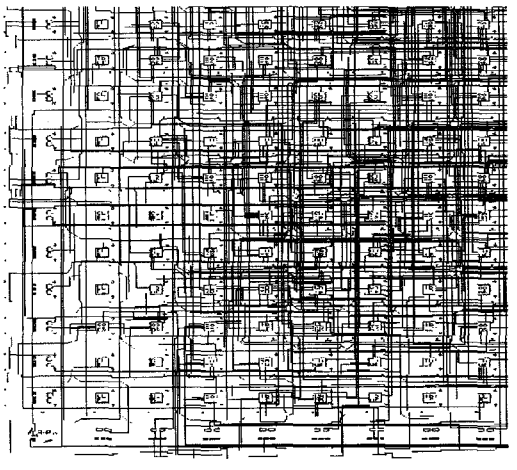

Figure 6 Partial layout of XC4006 ASIC for progressive VGA

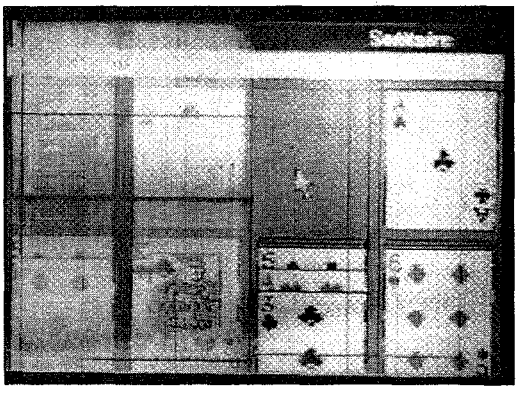

Figure 7(a) Photograph of projected image

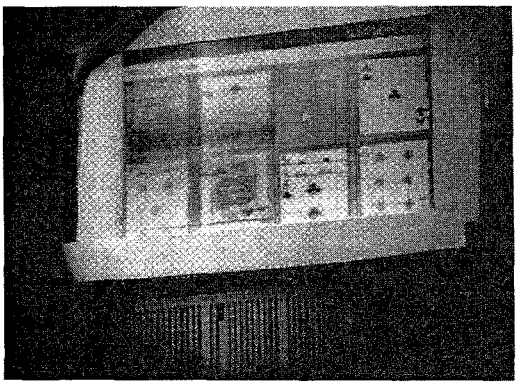

Figure 7(b) Photograph of direct-view image

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