32.3: Metal-Induced Unilaterally Crystallized Polycrystalline Silicon Thin-Film Transistor Technology for Active-Matrix Organic Light-Emitting Diode Displays with Reduced Susceptibility to Cross-Talk

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Abstract

In active-matrix organic light-emitting diode displays, a pixel in its non-emitting state is determined to be more sensitive to transistor leakage than one in its emitting state. An improved device design is proposed and implemented, employing gate-modulated lightly-doped drain to suppress transistor leakage and to improve image quality.

1. Introduction

Organic light-emitting diode (OLED) is challenging liquid-crystal (LC) as an alternative flat-panel display technology because of its ease of manufacturing due to its all solid-state nature and its relative merits of having a faster switching speed and being self-emitting with a wider viewing angle.

Unlike voltage-switched LC pixels, OLED pixels are current-driven. Consequently, OLED-based active-matrix (AM) displays require thin-film transistors (TFTs) capable of delivering high drive current (I_{on}) in the on-state. While it is feasible to implement pixel transistors in AM-LC displays using n-channel amorphous silicon (a-Si) TFTs with relatively poor device characteristics, p-channel polycrystalline silicon (poly-Si) TFTs capable of driving significantly higher I_{on} are required for implementing the pixel transistors in AM-OLED displays [1].

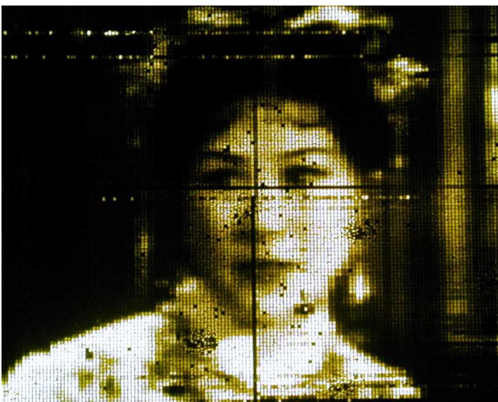


Figure 1. Typical image of a 160-by-120 AM-OLED display.

Metal-induced unilaterally crystallized (MIUC) poly-Si TFT technology [2] has been applied to implement AM-OLED displays (Fig. 1). While the brightness and uniformity of the two-transistor AM pixel (Fig. 2) is adequate, the display suffers from image quality degradation (Fig. 3) resulting from leakage current (I_{lk}) induced cross-talk [3]. It is presently shown that I_{lk}, particularly its sensitivity to gate-induced drain leakage (GIDL) mechanism, is mainly responsible for the cross-talk.

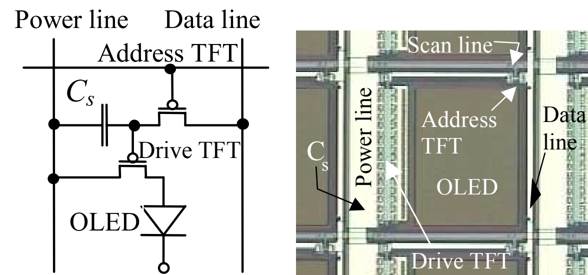
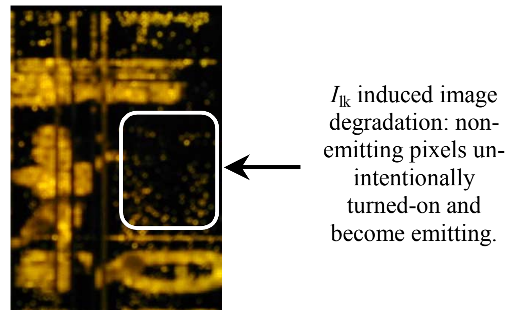


Figure 2. Circuit schematic (left) and photograph (right) of a two-transistor AM-OLED pixel.



I_{lk} induced image degradation: non-emitting pixels un-intentionally turned-on and become emitting.

Figure 3. Cross-talk induced image degradation in an AM-OLED display.

GIDL can be reduced by employing lightly-doped drain (LDD) or offset drain structures [4,5]. However, TFTs incorporating conventional LDD with oxide spacers or offset drains suffer from higher parasitic source/drain resistance. This leads to reduced I_{on}. An improved transistor design, in which the LDD is formed under poly-Si gate spacers, is presently proposed. The spacers are electrically connected to the gate. In the transistor "on" state, the LDD regions are accumulated and their resistance is lowered. This alleviates the negative impact of LDD resistance on I_{on}. In the "off" state, the regions are depleted and the carrier concentration is lowered due to the gate-modulation, thus their effectiveness in reducing the magnitude of any penetrating drain electric field is potentially enhanced

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2. Cross-Talk in OLED Pixels

Cross-talk among OLED pixels can be illustrated using the two pixels shown in Figure 4. Pixel P_1 is not being actively addressed ($V_{scan,\,1}$ is high), while Pixel P_2 is ($V_{scan,\,2}$ is low). The signal stored on C_s in P_1 is $V_{data,\,1}$ while that on the data line is $V_{data,\,2}$, to be written into P_2.

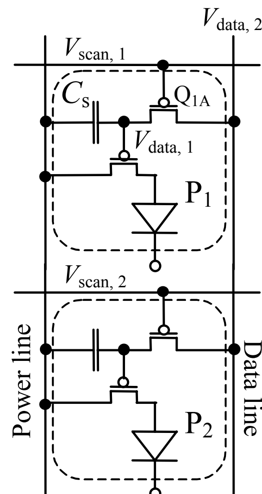

Figure 4. Circuit schematic illustrating leakage current induced cross-talk in an AM-OLED display.

Summarized in Table I are the possible cross-talk susceptible combinations of signal levels.

Table I. Cross-talk susceptible combinations of signal levels.

Pixel P_1: $V_{scan,\,1}$ = high	Pixel P_2: $V_{scan,\,2}$ = low
Non-emitting: $V_{data,\,1}$ = high	Emitting: $V_{data,\,2}$ = low
Emitting: $V_{data,\,1}$ = low	Non-emitting: $V_{data,\,2}$ = high

With P_1 non-emitting ($V_{data,\,1}$ high) and P_2 to be emitting ($V_{data,\,2}$ low), the C_s end of the p-channel address transistor (Q_{1A}) acts as the source. Finite I_{lk} through Q_{1A} causes $V_{data,\,1}$ to drop, thus making the effective gate drive ($V_{scan,\,1} - V_{data,\,1}$) on Q_{1A} more positive. If GIDL were severe, I_{lk} would increase. Such "positive feedback" mechanism results in $V_{data,\,1}$ being rapidly lowered. Consequently, a non-emitting pixel becomes emitting.

With P_1 emitting ($V_{data,\,1}$ low) and P_2 to be non-emitting ($V_{data,\,2}$ high), the "data line" end of Q_{1A} acts as the source. Finite I_{lk} through Q_{1A} causes $V_{data,\,1}$ to increase. However I_{lk} is insensitive to GIDL because $V_{data,\,2}$, hence the gate-drive on Q_{1A}, is fixed. Consequently, an emitting pixel is less susceptible to I_{lk}–induced cross-talk than a non-emitting pixel.

3. TFT Fabrication

A summary of the fabrication process for the realization of the MIUC TFT with gate-modulated (*gamo*) LDD is shown in Figure 5. The process began with the deposition and patterning of a 30nm thick a-Si active layer. 50nm thick low-temperature oxide (LTO) as the gate dielectric, 300nm a-Si as the gate electrode and 50nm LTO as an etch-step were next deposited. Following the gate electrode patterning, $1\text{x}10^{14}/\text{cm}^2$ boron ions were implanted to fix the doping concentration for the LDD. A layer of 500nm thick a-Si was deposited and anisotropically etched to form the spacers.

A crystallization-inducing hole was opened in the gate dielectric on one end of the transistor island. Nickel was evaporated before heat treatment at 500°C for metal-induced lateral crystallization [6]. Any excess nickel was removed prior to heavy source/drain boron implantation, at a dose of $4\text{x}10^{15}/\text{cm}^2$. After dopant activation at 500°C for 3hrs, 500nm LTO insulation layer was deposited. Contact holes were opened, 1µm Al deposited and patterned, before the transistor was sintered in Forming gas at 420°C for 0.5hr.

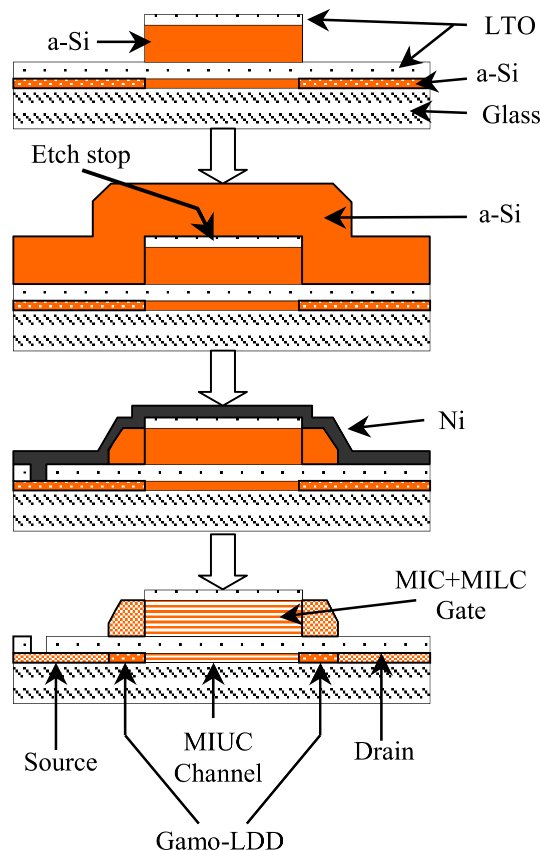

Figure 5. Schematic cross-sections showing the evolution of the structure of an MIUC TFT with *gamo*-LDD.

4. Device Characteristics and Simulation

The dependence of the drain current (I_d) on the gate voltage (V_g) of MIUC TFTs with and without *gamo*-LDD is shown in Figure 6. When V_g is positive, the devices are "off" in the accumulation state, hence $I_d = I_{lk}$. For the device without *gamo*-LDD, I_{lk} increases exponentially with V_g – thus indicating the presence of a strong GIDL effect. The fact that I_{lk} is relatively independent of V_g in the off-state clearly indicates that GIDL is effectively suppressed in the TFT with *gamo*-LDD, while still preserving a relatively high I_{on}.

A closer inspection of I_{lk} reveals that there are two valleys separated by a V_g difference of ΔV. I_{lk} climbs out of the first valley as a result of an increase in drain electric field induced by

a reduction in channel resistance due to accumulation. The second valley is reached when the carrier concentration, hence the resistance, of the LDD is gate-modulated to its most efficient drain field reduction state. Beyond the second valley, the LDD becomes inverted. The location of the maximum drain field shifts to the junction between the LDD and the heavily doped drain and I_{lk} again increases exponentially.

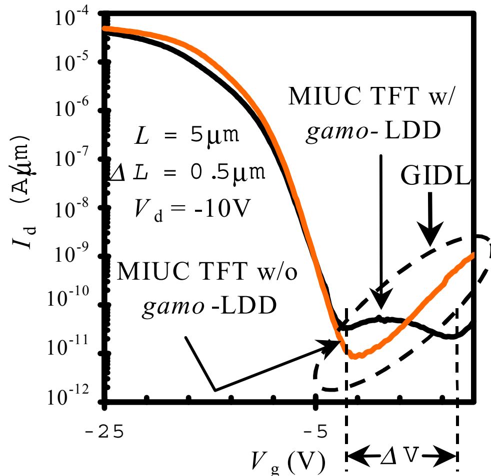

Figure 6. Transfer characteristics of MIUC TFT fabricated with and without *gamo*-LDD.

Shown in Figure 7 is the dependence of I_{lk} on V_d at a V_g of 10V for a conventional bilaterally crystallized MILC TFT and MIUC TFT with or without *gamo*-LDD. For I_{lk} to reach a value of 10pA/µm, the approximate V_d values sustained by the three TFTs are -2, -4, -10V, respectively. *Gamo*-LDD is clearly capable of significantly reducing GIDL. The dependence of ΔV on LDD implant dose is shown in Figure 8. While still preserving a small I_{lk}, the largest (hence the most optimal) ΔV is obtained at a dose of 1~ 2x10^{14}/cm^2.

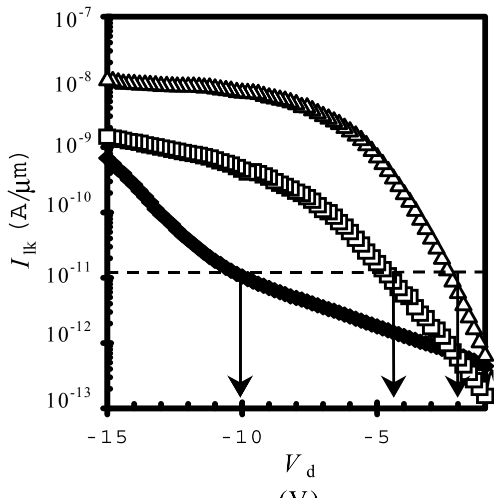

Figure 7. Dependence of I_{lk} on V_d of bilaterally crystallized MILC TFT (hollow triangle), MIUC TFT without (hollow square) and with *gamo*-LDD (filled diamond).

The dependence on V_g of the magnitude and location of the lateral electric field (E_x) in the drain/channel region for MIUC TFT without *gamo*-LDD and drain/LDD/channel region for MIUC TFT with *gamo*-LDD was studied using a device simulator and shown respectively in Figures 9 and 10. The dependence of the maximum E_x is summarized in Figure 11.

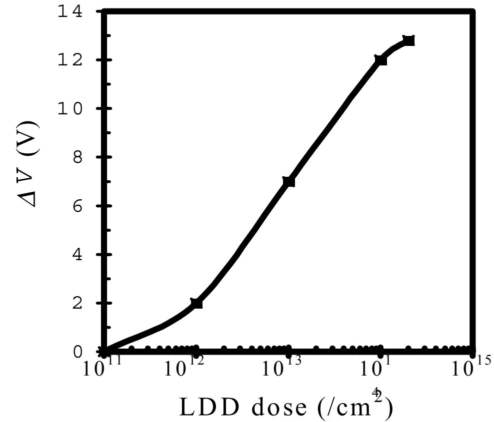

Figure 8. Dependence of ΔV on LDD implant dose.

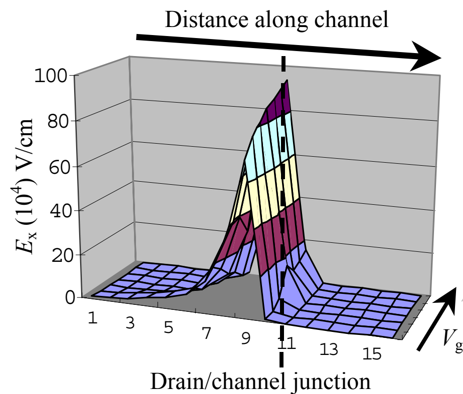

Figure 9. Dependence on V_g of the distribution of E_x in a conventional MIUC TFT without *gamo*-LDD.

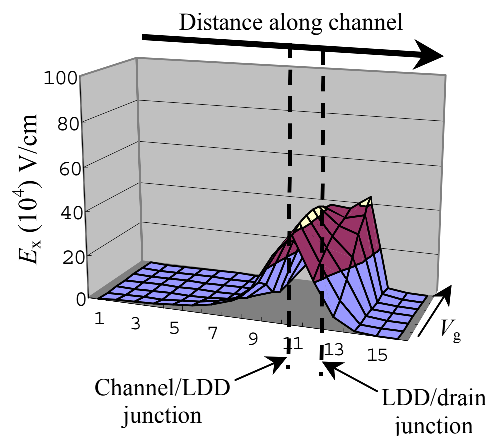

Figure 10. Dependence on V_g of the distribution of E_x in an MIUC TFT with *gamo*-LDD.

At a V_d of –12V, the maximum drain field ($E_{x,\ max}$) increases from ~0.6MV/cm at V_g = 0V to ~0.9MV/cm at V_g = 12V (Fig. 9) for the TFT without *gamo*-LDD. Whereas for the TFT with *gamo*-LDD, the location of $E_{x,\ max}$ shifts from the channel/LDD junction to the LDD/drain junction as V_g is increased from 0V to 12V while its magnitude is relatively unchanged at ~0.3 to ~0.4MV/cm.

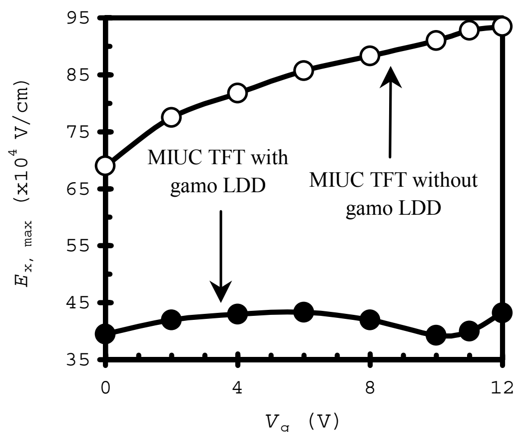

Figure 11. Dependence of $E_{x,\ max}$ on V_g.

It can be seen in Figure 11 that for the TFT with *gamo*-LDD, not only is the reduction in $E_{x,\ max}$ (hence I_{lk}) reproduced by the simulation but also its V_g dependence. The initial increase and subsequent decrease in the $E_{x,\ max}$ exactly mirror a similar dependence of I_{lk} on V_g shown in Figure 6.

The dependence of the maximum vertical electric field ($E_{y,\ max}$) on V_g is shown in Figure 12. It is also reduced in a TFT with *gamo*-LDD.

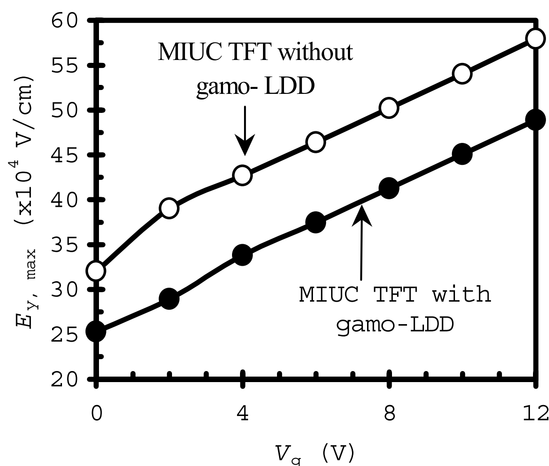

Figure 12. Dependence of $E_{y,\ max}$ on V_g.

5. Display Implementation

As a demonstration, AM-OLED displays using TFTs with or without *gamo*-LDD have been fabricated. The images are compared in Figure 13. It can be seen that the display implemented using TFTs without the I_{lk}-reducing *gamo*-LDD suffers from severe cross-talk induced image degradation. A large number of non-emitting pixels are unintentionally turn on and become emitting. The display implemented using TFTs with *gamo*-LDD is clearly superior and does not suffer from similar I_{lk}-induced image degradation.

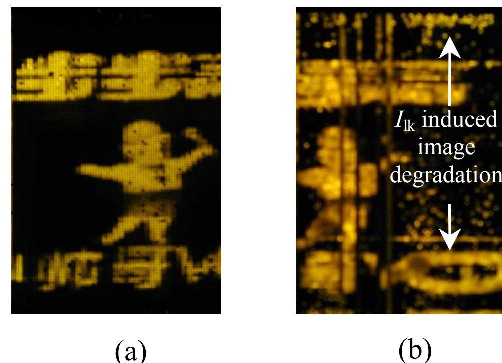

Figure 13. AM-OLED displays implemented using MIUC TFTs with (a) and without (b) *gamo*-LDD. I_{lk}-induced image degradation is clearly visible in (b).

6. Conclusion

Without excessive sacrifice of the on-state drive current, leakage current in low-temperature metal-induced unilaterally crystal-lized polycrystalline silicon thin-film transistors has been reduced by incorporating a *gate-modulated* lightly-doped drain structure. Such structure reduces the strength of the electric field near the drain/channel junction region. The leakage current is typically less than 50pA/µm at a V_d of -10V and a V_g of 10V. The new MIUC poly-Si TFTs are applicable to the realization of high quality AM-OLED displays and 3-dimensional integrated circuits.

7. Acknowledgment

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8. References

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