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Behavior of the drain leakage current in metal-induced laterally crystallized thin film transistors

Gururaj A. Bhat, Hoi S. Kwok, Man Wong *

Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

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Abstract

Although conventional metal-induced laterally crystallized (MILC) thin film transistors (TFTs) are better than solid phase crystallized (SPC) TFTs in many device performance measures, they are less ideal in others, owing to the higher leakage current and early drain breakdown. It has been found that degradation can be reduced by eliminating the overlap of the metallurgical junctions of the source/drain regions, formed by metal-induced crystallization (MIC), and the grain boundaries at the MIC/MILC interface. Here, the drain leakage current (I_{lk}) behavior of MILC TFTs with and without overlap has been studied. It is observed that under certain gate bias conditions, the relative magnitude of I_{lk} for the two kinds of devices exhibits an interesting reversal as the drain bias is varied.

Keywords: Thin film transistors; Leakage current; Metal induced crystallization

1. Introduction

High mobility polycrystalline silicon (poly-Si) thin film transistors (TFTs) with a low leakage current are desirable for integrating driver circuits and pixel transistors on the same glass panel for active matrix liquid crystal displays (AMLCDs). Although solid phase crystallized (SPC) is a relatively inexpensive batch process, its processing temperature at around 600°C still exceeds the upper processing temperature limit of the inexpensive glass substrates popularly used for liquid crystal displays (LCDs). Recently, a low temperature (~500°C) metal-induced-lateral crystallization (MILC) technique for poly-Si has been proposed [1]. Although the resulting TFTs have been shown to possess excellent device characteristics because of the longitudinal grains in the active channels [2], they are less ideal in others, such as exhibiting higher drain leakage current (I_{lk}) [3] and earlier drain breakdown [4].

Because metal-induced crystallization (MIC) occurs in the source and drain regions of the conventional MILC TFTs, continuous MIC/MILC interfacial grain boundaries (MMGBs) [5] are formed at the source and drain ends of the MILC channels. In TFTs employing self-aligned source and drain doping, these MMGBs fall within the depletion regions of the metallurgical junctions and degrades the I_{lk} behavior of the TFTs. In this work, the I_{lk} behavior of TFTs with and without the MMGB/junction overlap has been characterized. Under certain gate bias conditions, the relative magnitudes of I_{lk} for the two kinds of devices have been observed to exhibit an interesting reversal as the drain bias is varied.

2. Experimental

Four-inch silicon wafers covered with a 100 nm thick thermal oxide were used as the starting substrates. A thin 100 nm amorphous silicon (a-Si) layer was first deposited by low-pressure chemical vapor deposition (LPCVD) at a pressure and temperature of 300 mTorr and 550°C, respectively. After patterning of the a-Si layer into active islands, a 100 nm thick layer of LPCVD

* Corresponding author. Tel.: +852-2358-7057; fax: +852-2358-1485.

E-mail address: eemwong@ee.ust.hk (M. Wong).

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low temperature oxide (LTO) gate insulator and 200 nm thick a-Si gate electrode were deposited. The wafers were thoroughly cleaned after the gate etching and the exposure of the source and drain regions. About 2 nm of Ni was deposited in an ultra-high vacuum evaporation system. For those TFTs with an offset (5 μm) between the edges of the gate and the evaporated Ni, an additional lithographic step for patterned Ni deposition was carried out before the Ni evaporation. Subsequently, the source, drain, and gate regions were doped by self-aligned phosphorus implantation at a dose of 3×10^{15}/cm^2 and an energy of 40 keV. The wafers were then heat treated at 500°C for 9 h, during which simultaneous Ni induced crystallization of the a-Si layers and dopant activation were accomplished. Finally, contact holes were opened through 500 nm of the LTO insulation layer, Al-1%Si was sputter deposited, and the devices were sintered in forming gas at 400°C for 30 min.

3. Results and discussion

The transfer characteristics of the two kinds of devices (Fig. 1) are shown in Fig. 2, where "oMILC" denotes MILC TFTs with offsets between the MMGBs and the junctions, and "cMILC" denotes conventional MILC TFTs with MMGBs self-aligned to the metallurgical junctions between the channel and the source and drain regions. Besides exhibiting a faster subthreshold turn on, the oMILC TFTs also show a tighter distribution of lower threshold voltage (V_{th}) values (Fig. 3).

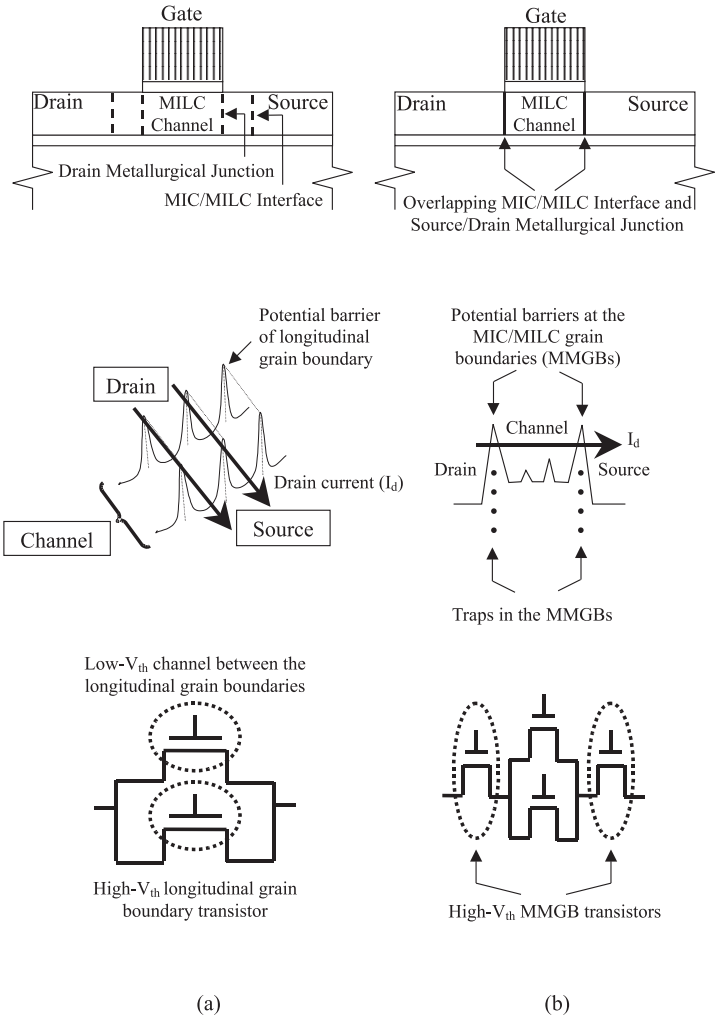

Fig. 1. Schematics of oMILC and cMILC TFTs. Also shown are grain boundary models and the low V_d transistor models of (a) oMILC TFT and (b) cMILC TFT.

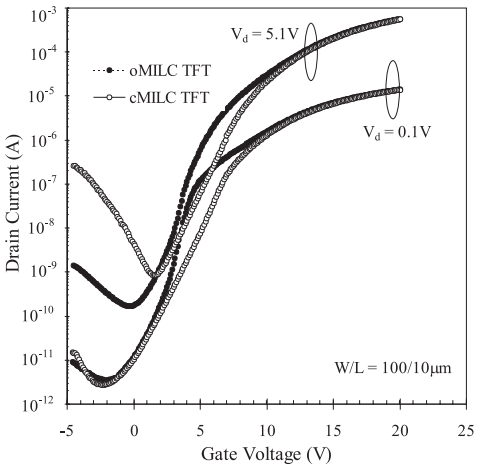

Fig. 2. Comparison of the transfer characteristics of oMILC and cMILC TFT.

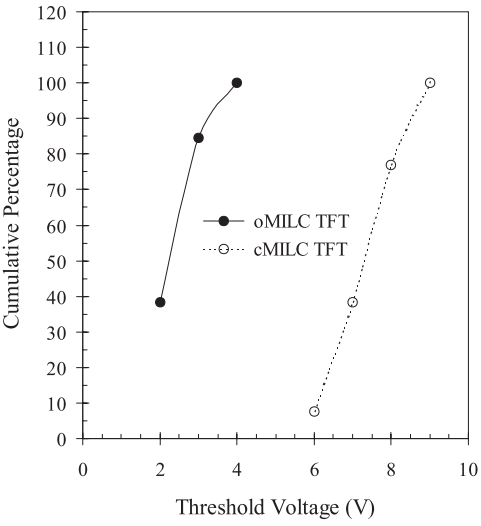

Fig. 3. Plot of cumulative % distribution of the threshold voltage of oMILC and cMILC TFTs.

It can be seen that when $-3\ V < V_g < 0\ V$, I_{lk} at low V_d (0.1 V) for the cMILC TFTs is smaller than that for the oMILC TFTs. This is because of the relatively narrow gate induced depletion region width in the gate–drain overlap region at small negative V_g. Consequently, I_{lk} is limited by the overall channel resistance.

The channel resistance is higher in cMILC TFTs because the higher density of MMGB traps raises the "V_{th}" of the MMGB TFTs near the drain and source ends of the channel (Fig. 1b). This effectively increases the V_{th} (Fig. 3) of the overall device, which is defined as the V_g required to achieve a normalized drain current (I_d) of $(W/L) \times 10$ nA at $V_d = 0.1\ V$.

As the magnitude of the negative V_g is increased, the gate induced depletion region widens and I_{lk} becomes dominated by the trap-assisted thermal generation current [6]. Because of the presence of an MMGB in the drain metallurgical junction, I_{lk} for the cMILC TFTs is enhanced by the high density of MMGB traps [4] and overtakes I_{lk} for the oMILC TFTs.

No I_{lk} cross-over is observed at a high V_d (5.1 V), with I_{lk} always higher in the cMILC TFTs. This is because I_{lk} at a high V_d is dominated by the trap-assisted field emission current [7] and the overlap of the defective MMGB and the high field at the drain metallurgical junctions in cMILC TFTs naturally leads to a higher I_{lk}.

An alternative way of looking at this is presented in Fig. 4. It is obvious that when V_g is −5 V, I_{lk} in cMILC TFTs is always higher, being dominated by thermal generation and trap-assisted field emission at low and high V_d, respectively. On the contrary, when V_g is 0 V, the relative magnitudes of I_{lk} for the two kinds of TFTs exhibit an interesting reversal as the drain bias is increased. In summary, I_{lk} is lower for cMILC at a low V_d because of the higher effective channel resistance and higher at a high V_d because of trap-assisted field emission.

It should be noted that the difference in the effective V_{th} shown in Fig. 3 is only apparent [8] and does not lead to an increase in I_d at a sufficiently high V_g. This is because the definition of V_{th} adopted here is different from the conventional V_{th} obtained by extrapolating from the linear regime of the I_d–V_g characteristics.

When an MMGB coincides with any one of the metallurgical junctions, it becomes a part of the channel. The high density of grain boundary trap states effectively raises the V_{th} of the region of the device, where an MMGB is located. However, since an MMGB has a very small lateral extent, it can be considered as a device

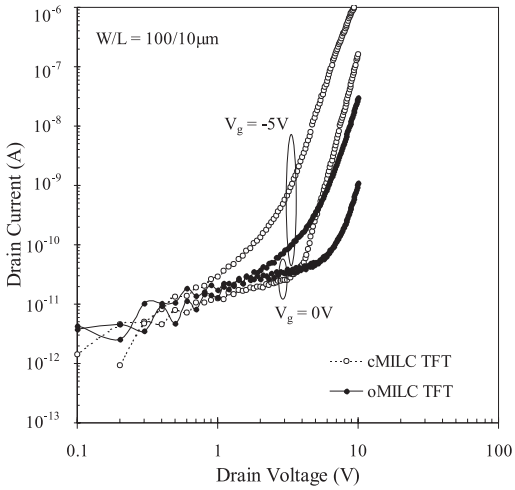

Fig. 4. Dependence of the leakage current of oMILC and cMILC TFTs on drain bias, at two different gate bias conditions.

with a very short channel length, albeit with a higher V_{th}. Although conduction at a low V_g is limited by the high V_{th} MMGB TFT, it is limited at a high V_g by the resistance of the intrinsic MILC "long" channel TFT (Fig. 1a), which is common to both the cMILC and the oMILC TFTs. Consequently, the linearly extrapolated V_{th} of the two kinds of devices would be the same.

4. Conclusion

The presence of the MMGB/metallurgical junction overlap is directly responsible for the higher I_{lk} and threshold voltage in cMILC TFTs. The removal of the overlap results in a reduced I_{lk} and a lower threshold voltage. I_{lk} is always higher in cMILC TFTs at a high V_d because of trap-assisted field emission. At a low V_d, I_{lk} in cMILC TFTs is lower at a smaller negative V_g because of the higher effective channel resistance.

Acknowledgements

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