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Cost-effective Driving Scheme for Bistable Cholesteric Displays

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For VLSI implementation, low operation voltage and switching current are the major concerns. Yet, none of the driving schemes published so far has addressed this combined issue. We studied the electro-optic characteristics of bistable cholesteric displays at the low transition voltage in this paper, and the effect of slew-rate on the maximum output current and average output power in a forthcoming paper. The dynamic responses were measured and an efficient scheme was devised accordingly. The most cost-effective addressing time was 4 ms/line using the low-end twist nematic (TN) or super twist nematic (STN) mixtures.

KEYWORDS: bistable cholesteric display, driving scheme, electro-optic

1. Introduction

Bistable cholesteric displays (BCD) are known to have two stable states even the applied electric field is removed. These states are often referred to as the planar and focal-conic states in accordance with the optical properties. The bright appearance at the planar state is due to the selective Bragg reflection of the ambient light induced by the periodic helical structures. It can in principle reflect as much as 50% of the ambient light within a certain spectral bandwidth. The reflectance associated with the planar state depends on the birefringence of liquid crystal mixtures, cell gap and anchoring conditions.[1–3] To broaden the viewing angle, polymer network formed in the liquid crystal medium has been demonstrated but the principle of operation is the same with the typical operation voltage of $80V_{pp}$. On contrary, the helical axes distribute randomly in the focal-conic state so that the light is weakly scattered in the forward and backward directions. By putting black paint at the rear glass surface of BCD, the focal-conic state will appear dark giving rise to a good contrast. It is thus advantageous for the display applications that require high multiplexibility and low power consumption. As the stringent cell gap control and polarizer laminations are not required, it will simplify a lot of the manufacturing processes.

Nevertheless, to reduce the addressing time per line, special driving schemes such as those proposed by the researchers at Kent State University are necessary.[4–7] To address a single pixel, they use a driving waveform composed of at least 3 stages (preparation, selection and evolution) of several tens of milli-seconds. Thus, it will require a composite waveform to appear in the data stream if the voltage is to be shared equally between the row and column drivers. Alternatively, to minimize the circuit complexity, a nearly full drive voltage is to be provided by the row driver in their schemes. In addition, the switching current per pixel may become excessive high if rapid addressing pulses less than 1 ms are to occur in every addressing cycle. On the other hand, the researchers at Minolta[8] have also proposed a driving scheme for the stacked multicolour BCD. They use high voltage pulses to select the planar state and the initial state is always focal-conic. These are in contrast with our case where low voltage pulses for the focal-conic state selection and initial planar state are chosen. So basically their scheme is the reverse operation mode of ours.[9,10] In this paper, we shall study the electro-optic characteristics and show the possibility to operate the BCD at the pixel voltage shared equally by the row and column drivers or the row driver only. This reduces the maximum drive voltage by half. We also find that for the low-end nematic mixtures, the most cost-effective addressing time is 4 ms/line. If the addressing time is shorter than 1 ms per line for example, more than 20% increase in the drive voltage is required. This trend is universal for the root-mean-square (rms) based addressing schemes. We shall compare the tradeoffs between 2 ms/line and 4 ms/line addressing in our forthcoming paper. The driving scheme is described in §2 and the electro-optic characteristics are shown in §3.

2. Driving Scheme

In our scheme, the rule to address BCD is to clear-before-write the data. The clearing time is denoted by t_c while the writing time is t_w. To generalize the discussion, the peak voltage of either row or column is set to 0.5 so that the voltage across a pixel can be 1 during t_c. With respect to the row voltage, the data voltage for the planar to focal-conic state transition (OFF) is 180° out of phase during t_w. Whereas they are in phase to maintain the planar state (ON). In other words, the phase relation is used for the voltage addition or subtraction. Since it is first cleared, there is always a growing planar state at the beginning of each addressing cycle after t_c, in comparison with those in refs. 4–7 that it can happen at the last row of the display. The pipeline algorithm is commonly used to minimize this shortcoming. The waveforms to turn on or off a pixel are depicted in Fig. 1, where R_i, C_j and P_{ij} are the ith row, jth column and (i, j) pixel respectively. Therefore, the voltages for both states are given by the following equation

$$r_F = 0.5 + r$$
$$r_P = 0.5 - r \quad (1)$$

where the suffix represents the planar or focal-conic state and r denotes the data voltage. All voltages are quoted in the peak-to-peak value and are normalized with respect to the drive voltage. The choice of 0.5 for the row voltage is primarily due to the simplification in the row driver design and will be tested for a certain t_w. Other factors that determine the electro-optic characteristics are t_c, r and t_w and will be discussed in the next section. Since the pixel voltage in this scheme is controlled by the phase relationship of data voltage, its rms value is always a constant regardless of the displayed pattern. Consequently, the problem associated with the indeterministic rms data voltage in our previous publications[9,10] can be solved. In addition, the clearing voltage can be provided by a single row driver since only the out of phase condition is to meet at the row and column during t_c. It thus minimizes the non-

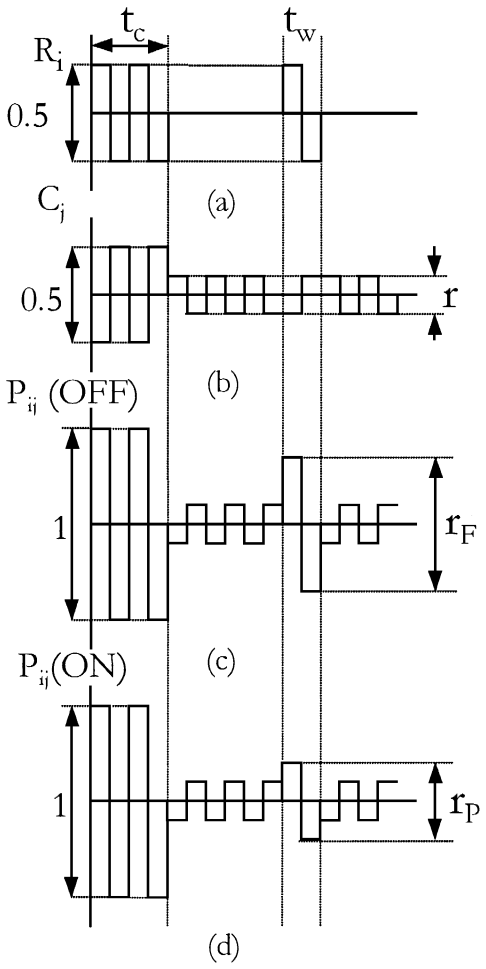


Fig. 1. Waveforms proposed to turn on (in phase) or off (out of phase) a pixel of BCD.

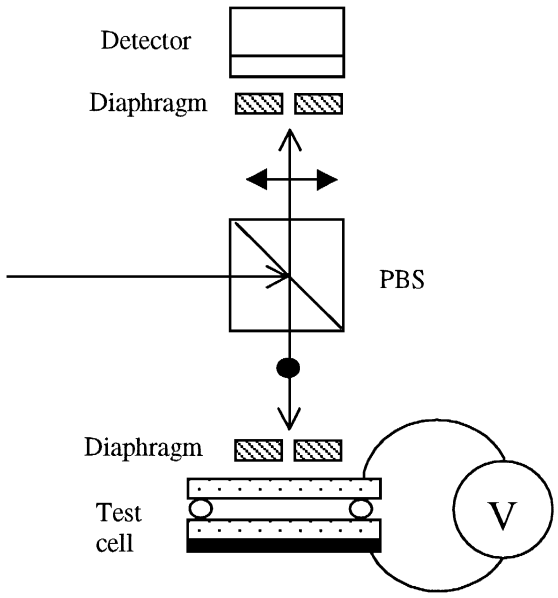


Fig. 2. Experimental setup for the measurements of the reflectance and dynamic responses.

standard cells fabricated on the same IC die and any parasitic couplings caused.

3. Results and Discussions

For the measurement discussed in this section, a batch of test cells was fabricated in our laboratory. Unrubbed polyimide PIA3744 from Chisso Corp. was coated on the indium tin oxide (ITO) glass surface and low-cost nematic mixture DLC-42121 from Dainippon Ink & Chemicals Inc. was used. The cell gap was about 4 μm and the cell reflected 543.5 nm laser light. To reduce the Fresnel reflections, the electro-optic characteristics were measured in a cross-polarization setup shown in Fig. 2. The p-wave was reflected by the polarized beam splitter (PBS) and incident normal to the test cell. The s-wave of the circularly polarized light reflected from the cholesteric helical structures was transmitted and detected by a silicon photo-detector. Voltage signal can be acquired and integrated real-time by the Hewlett-Packard Infinium Oscilloscope. Hence the reflectance and the dynamic responses can be measured accordingly. The p- and s-waves were represented by the dot and arrow respectively. The PBS was broadband and purchased from Newport Corp.

3.1 Effect of t_c, r and t_w

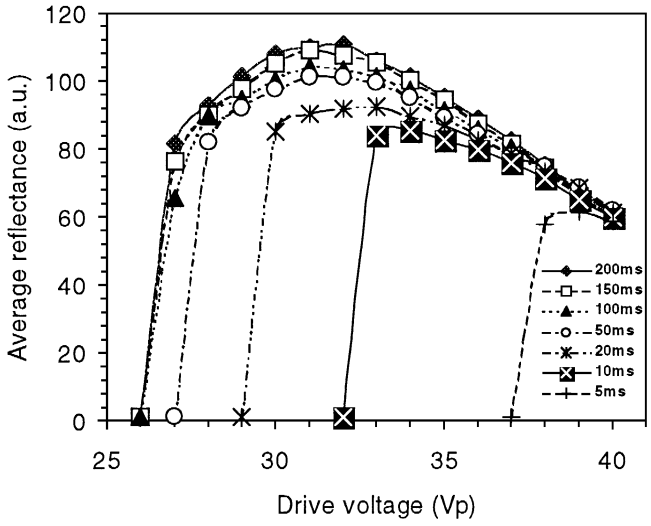
A waveform similar to that in Fig. 1(b) with the clearing voltage set to 1 instead was applied to the test cell. The average reflectance was measured and it showed a strong dependence on the clearing time [Fig. 3(a)]. The drive voltage to achieve an attainable reflectance for $t_c = 20$ ms was about $30V_{peak}$. The shift in the on-set of reflectance was due to the rms requirement to deform the liquid crystal molecules homeotropically. The downfall on the high voltage side was caused by the increasing influence of data voltage at the signal floor. This trend also happened in the following measurements. To show a good indication of the final reflectance, the average reflectance $\langle R \rangle$ in this section was defined as

$$\langle R \rangle = \frac{1}{T - t_c} \int_{t_c}^{T} R dt \qquad (2)$$

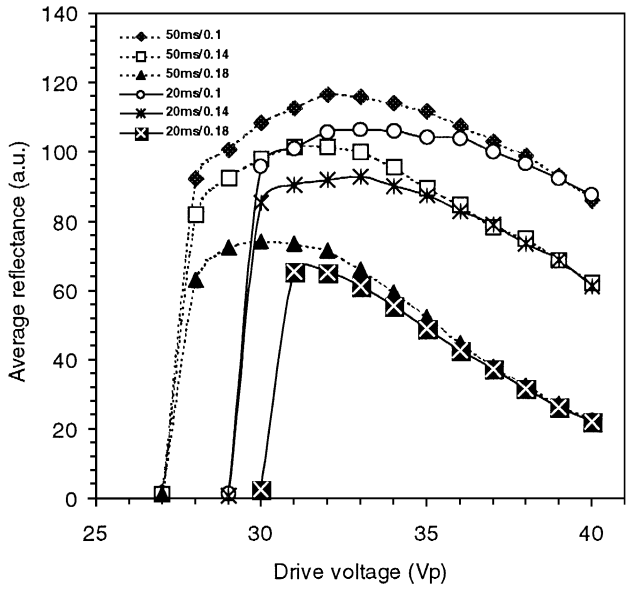
where the period T equal to one second was used in the calculation.

In Fig. 3(b), the effect of data voltage r was studied for two different clearing times. Lower data voltage led to higher reflectance but less control in state selection [see eq. (1)], and vice versa. We chose to work close to $r = 0.14$ since it depended on the threshold of planar to focal-conic state transition. This dependence is a characteristic of upsetting the regular helical axis orientation in the planar cholesterics, and it does not vary much for typical Twist Nematic or Super Twist Nematic mixtures. Therefore 20 ms clearing time is sufficient at the drive voltage of $34V_{peak}$.

On applying bipolar pulses of duration t_w to the cell, the corresponding hysteresis of reflectance was plotted in Fig. 4. The black and white symbols represented the incremental and decremental cycles respectively. The frequency of pulses was 1 kHz and the period was one second. There was also about one second delay between the bipolar pulses and the reflectance measurement. To initialize to the same reflectance at zero voltage, a large ac voltage of 1 kHz was applied between the successive series of measurements. On the high voltage side, the reflectance was lower than the initial value and it decreased as the pulse amplitude increased. This could be understood as the non-negligible shear flow effect occurred at the high field.[11,12] It would alter the final helical axis distribution and hence the reflectance.[1–3] Nevertheless, this high



(a)



(b)

Fig. 3. Average reflectance (a) at different clearing time t_c with $r = 0.14$, and (b) at different data voltage r with $t_c = 20$ ms and 50 ms. In both cases, the frequency is 1 kHz and the period of measurement is 1 s.

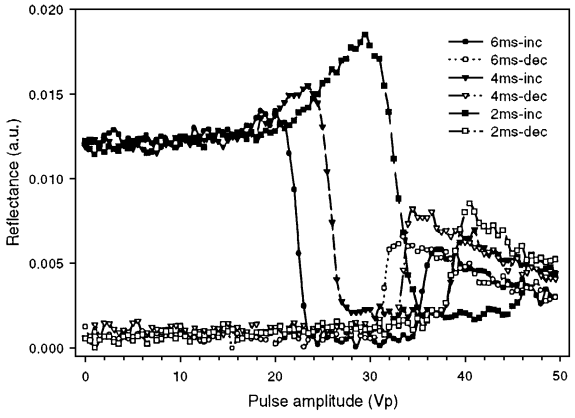
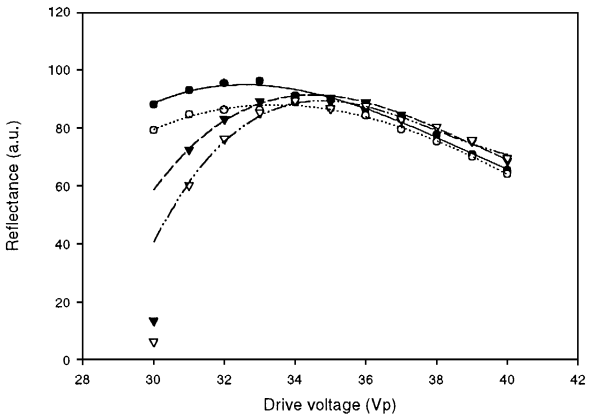


Fig. 4. Reflectance against pulse amplitude at different writing time. The incremental and decremental voltages are deno ted by *inc* and *dec* respectively. The period and the delay before measurement are 1 s while the frequency is 1 kHz.

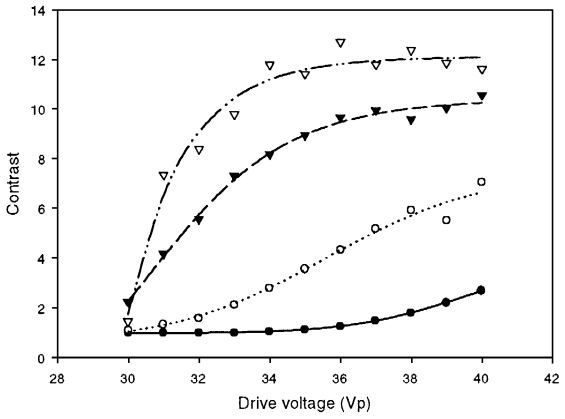
field pulses could be used for the gray-level control. On the low voltage side, the peak due to well-aligned helical domains shifted right as the duration t_w became shorter. The quiescent point where the reflectance was about half the initial value also changed in the same fashion. It was clear that such shift was not linear as the writing time became shorter, even there was no influence due to the floor voltage. The ultimate choice of addressing time would thus be determined by this voltage shift and be constrained by the maximum allowable supply voltage. For $t_w = 4$ ms, this quiescent point occurred at about $25V_{peak}$ which corresponded to 0.735 at the drive voltage equal to $34V_{peak}$. It was nearly 50% more than the value 0.5 proposed in §2. However, with the aids of the data voltage $r = 0.14$, which was close to the planar to focal-conic transition threshold at the above drive voltage, we were able to demonstrate this operation in the next part.

3.2 Dynamic response

As mentioned in §2, once r was determined the other voltages would be fixed according to eq. (1). Thus $r_F = 0.64$, $r_P = 0.36$ and $r = 0.14$ were used in the following measurements. In Fig. 5, the reflectance and contrast were mea-



(a)

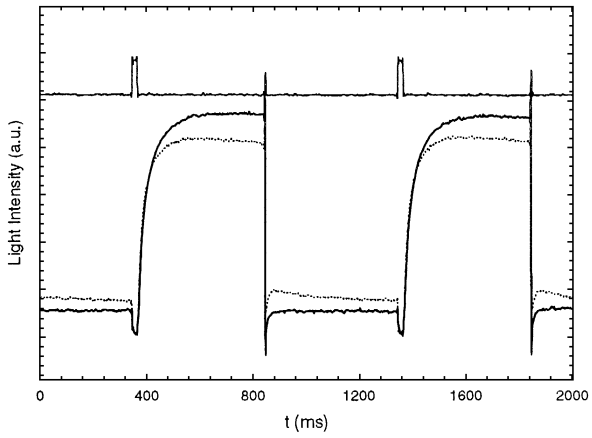


(b)

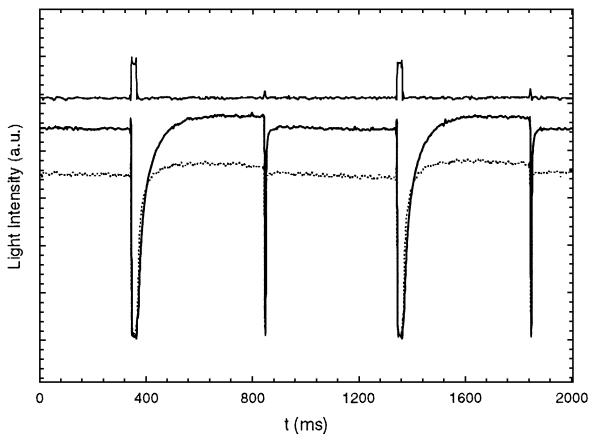
Fig. 5. (a) Reflectance measured as the steady response at the planar state and (b) contrast calculated using the steady responses at the planar and focal-conic states. In both cases, 20 ms clearing time, 0.14 data voltage and 1 kHz frequency are used. All plots vary with different writing time: 1 ms (solid circle), 2 ms (hollow circle), 4 ms (solid triangle) and 6 ms (hollow triangle).

sured dynamically (see Fig. 6 as well). During each period of 1 s, the reflectance was determined as the steady response at the planar state. Meanwhile together with the response at the focal-conic state, the contrast was calculated. The choice of 2 ms resulted in a nearly unchange in the reflectance, whereas that of 6 ms showed a higher contrast ratio. Compromised reflectance and contrast occurred at $34V_{peak}$ and $t_w = 4$ ms.

The dynamic responses based on our scheme were shown in Fig. 6. It was noted that due to the low sampling rate, only the envelope of the waveform proposed in §2 was shown. The input waveform for 2 ms case was not plotted for clarity. Higher drive voltage of $37V_{peak}$ was necessary to obtain satisfactory contrast and reflectance when t_w was reduced from 4 ms to 2 ms. Further development in optimizing the liquid crystal response should bring closer the electro-optic performance between 2 ms/line and 4 ms/line addressing. Choosing the later was based on the material cost and electrical requirement arguments. To display a text of a thousand lines per second, we may combine 2 ms/line addressing and the dual scan technique. Addressing time shorter than 1 ms is bounded by more than 20% increase in drive voltage, and according to our studies in the current and power requirements, short pulses are to add cost to the fabrication processes and reliability issues. Like other schemes, there is also a noticeable change in the reflectance at the beginning of each addressing cycle. This shortcoming is intrinsic if the homeotropic state is intermediate between the state transitions.



(a)



(b)

Fig. 6. Dynamic response of the reflectance (a) when the focal-conic state (OFF) is addressed and (b) when the planar state (ON) is maintained. The solid and dotted lines represent $t_w = 4$ ms and $t_w = 2$ ms respectively. Correspondingly, the drive voltages are $34V_{peak}$ and $37V_{peak}$. In both cases, 20 ms clearing time, 0.14 data voltage and 1 kHz frequency are used.

4. Conclusions

We demonstrated that based on our simple scheme the drive voltage could be shared in half by the row and column drivers or the row driver only. This already divided the maximum output current into equal halves that relaxed the current requirement. Best electro-optic characteristics could be obtained for 4 ms/line addressing using the low-end mixtures. All these together with the deterministic data voltage and short clearing time were the major differences compared with our patent and publication.[9,10]

Acknowledgement

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