Analysis and Reduction of Kink Effect in MILC-TFTs

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Abstract

Impact ionization is the main cause of the kink effect in the saturation region of the output characteristics of the field effect transistors. In thin film transistors (TFTs) the kink effect is enhanced due to the presence of traps. The larger the number of traps, the larger the kink effect at a given drain bias. It is observed that the kink effect in conventional metal induced laterally crystal-lized (cMILC)-TFTs occurs at a lower drain bias than that in solid phase crystallized (SPC)-TFTs under the same gate drive. This is shown to result from the overlapping of the MIC/MILC interface and the drain metallurgical junction. Conse-quently, the kink effect can be reduced by eliminating the overlap.

Introduction

High mobility, low leakage and low temperature polycrystalline silicon (poly-Si) TFTs are in demand because they enable integration of the driver circuits with the pixel transistors on the same glass panel for large area electronics. Among the crystallization techniques such as SPC, excimer laser crystallization and rapid thermal crystallization, SPC has been the most widely used. Though SPC-TFTs have sufficiently high mobility for building driver circuits, they suffer from high leakage current and poor output characteristics. The reason for the inadequate device performance is the presence of both inter- and intra-granular trap states in the intrinsically defective poly-Si material. Yet another disadvantage of SPC is the relatively higher optimal processing temperature of around 600^{o}C. An alternative method of metal induced crystal-lization (MIC) of amorphous silicon (a-Si) at 500^{o}C has been proposed [1,2]. In order to prevent excessive metal contamination in the channel of the device, MILC is preferred. In general MILC-TFTs have exhibited better device performance than SPC-TFTs due to the presence of large longitudinal grains with lower defect densities [3] in the MILC poly-Si thin films.

Poor saturation behavior in poly-Si TFTs is due to the kink effect, which is an anomalous increase in drain current. It affects the maximum gain attainable in analog circuits and the power dissipation in digital circuits. In poly-Si TFTs, trap assisted field emission may dominate over impact ionization and the generated holes are most likely trapped in the defect states. As a result, poly-Si TFTs have been observed to exhibit more severe kink effect than bulk or silicon-on-insulator devices. Due to the better material quality of MILC thin films, one would expect the kink effect to be less

severe in MILC- than in SPC-TFTs. However, it can be deduced from our data that the overlapping of the MIC/MILC interface and the metallurgical drain junction in MILC-TFTs has a profound influence on the kink effect and that the effect can be reduced by separating the interface and the junction.

Experimental

Four-inch silicon wafers covered with 100nm thick thermal oxide were used as the starting substrates. A thin 100nm a-Si layer was first deposited by low-pressure chemical vapor deposition (LPCVD) at respective pressure and temperature of 300mtorr and 550^0C. After patterning the a-Si layer to form the active islands, a 100nm thick layer of LPCVD low temperature oxide gate insulator and 200nm thick a-Si layer gate electrode were deposited. The wafers were thoroughly cleaned after the gate patterning and the exposure of the source and drain regions. About 2nm of Ni metal was evaporated in an ultra-high vacuum system, before the source, drain, and gate regions were doped by self-aligned phosphorus implantation at a dose of $3x10^{15}/cm^2$ and an energy of 40keV. Devices with an offset between the gate edge and Ni were fabricated by using an additional lift-off mask to pattern the Ni. Subsequently, the devices were heat-treated at 500^0C for 9 hours, during which Ni induced crystallization of the a-Si layer and activation of the implanted dopants were accomplished simultaneously. No attempt was made to remove any remaining Ni metal after the MILC. Finally, after contact patterning and Al-1%Si sputtering, devices were sintered in Forming gas at 400^0C for 30 minutes. For comparison, devices were also fabricated using SPC at 625^0C for 10 hours. The schematic diagrams of MILC-TFT without and with the Ni-offset are shown in Figures 1a and 1b, respectively.

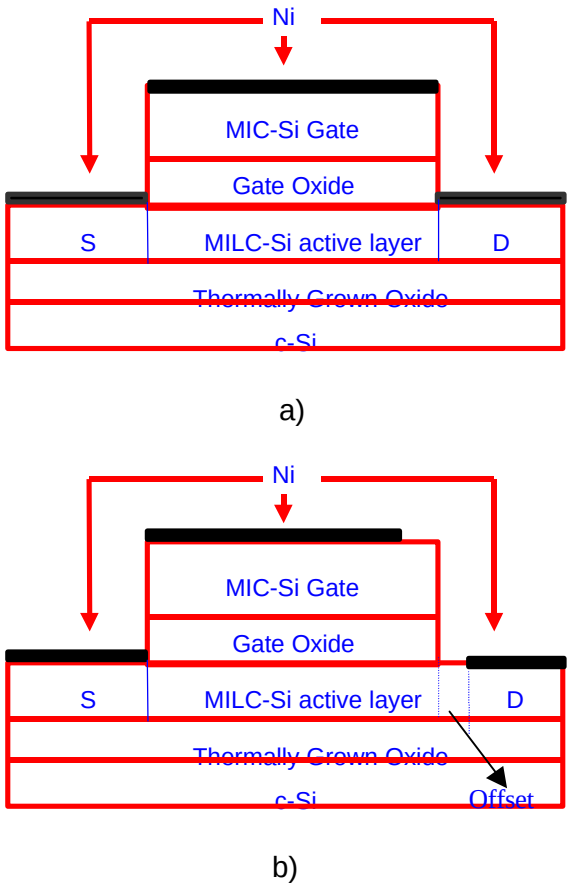
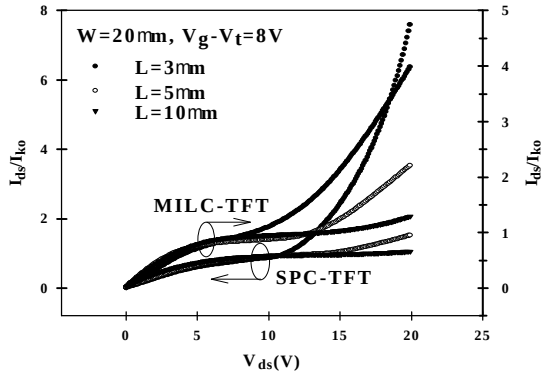


Figure 1. Schematic diagram of MILC-TFTs a) without b) with the Ni offset.

Output characteristics of the devices with channel lengths down to 3μm were measured. In order to take into account the difference in the channel lengths in MILC-TFTs and SPC-TFTs [4], the drain current is normalized to that (I_{ko}) at the onset of kink and in order to take different current levels

into account, output characteristics were obtained at common gate drive, as shown in Figure 2.



Fiure 2. Normalized output current characteristics of cMILC- and SPC-TFTs at common gate drive. 'I_{ko}' is the drain current at the onset of kink effect.

Results and discussion

The onset of the kink current in MILC-TFT is expected to occur at higher drain biases as compared to that in SPC-TFT. This is because the lower the trap density, the lower will be the kink effect in polysilicon TFTs [5]. However, as shown in Figure 2, though kink effect in cMILC-TFT has similar dependence on channel length as in SPC-TFT, the onset of kink in cMILC-TFT occurs at smaller drain biases and is more severe than that in SPC-TFTs. This is contrary to conventional expectations. We believe this happens due to the overlapping of MIC/MILC interface with the drain metallurgical junction. Mechanisms such as field emission via grain boundary traps and emission via metal precipitates will initiate increase in the output current at a field lower than that required for impact ionization [6]. It is well known that the lateral electric field peaks at the drain junction and the modulation of grain boundary barrier by the drain bias at the drain depletion region has a great influence on the trap assisted drain current in saturation region. The situation is more complicated in cMILC-TFTs than in SPC-TFTs, because of the overlapping of the MIC/MILC interface with the drain junction where drain electric field peaks, all along the channel width of the device.

A method [7] has been employed to separate MIC/MILC interface away from drain junction by offsetting the Ni deposition from the drain junction as shown in Figure 1b. This implies that upon Ni-induced crystallization, the grain boundary at the MIC/MILC interface, together with metal precipitates at this interface, will be separated from the drain metallurgical junction.

The output characteristics of conventional cMILC-, and offset oMILC TFTs are compared in Figure 3.

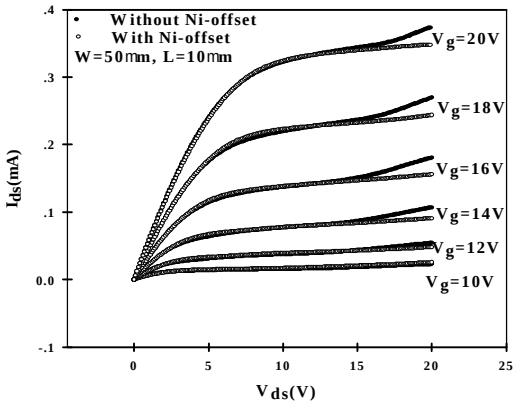


Figure 3. Output characteristics of cMILC- and oMILC-TFT.

Two sets of output characteristics of the devices with (oMILC) and without the Ni offset (cMILC) with 10μm channel length are shown. The Ni-offset is about 5 μm on the drain side. It can be observed that the kink is greatly reduced in the oMILC-TFTs. This is because only the longitudinal grain boundaries remain in the drain depletion region and increase in drain current due to lowering of the grain boundary barrier with drain bias and its exponential dependence on the drain voltage are greatly reduced.

Conclusion

Contrary to expectation the kink effect is much more severe in cMILC-TFTs than that in corresponding SPC-TFT. This is due to the overlapping of grain boundary at the MIC/MILC interface and the drain metallurgical junction all along the width of the device. By separating this interface away from the drain junction, kink effect is reduced.

Acknowledgment

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