Reverse Short-Channel Effect in Metal-Induced Laterally Crystallized Polysilicon Thin-Film Transistors

Man Wong, Gururaj A. Bhat, and Hoi S. Kwok

***Abstract*— A reverse short-channel effect, manifested by an increase in the transistor threshold voltage as the channel length is reduced, is observed in conventional metal-induced laterally crystallized thin-film transistors. Such an effect has not been observed in regular solid phase crystallized thin-film transistors and can be eliminated by a brief hydrogen plasma treatment.**

***Index Terms*—MILC, short channel effect, thin film transistor.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (TFT's) with high field effect mobility and low leakage current are required for realizing active matrix liquid crystal displays (AMLCD's) with integrated peripheral circuits and pixel switches. Although solid phase crystallization (SPC) is a relatively inexpensive batch process, its processing temperature at around 600 °C still exceeds the upper temperature limit of the inexpensive glass substrates popularly used for LCD's. An alternative low-temperature (∼500 °C) crystallization process using metal-induced lateral crystallization (MILC) has been proposed [1], resulting in TFT's with excellent device properties because of the longitudinal grains in the active channels [2].

Because metal-induced crystallization (MIC), instead of MILC, occurs in the source and drain (S/D) regions of conventional MILC TFT's, continuous MIC/MILC interfacial grain boundaries (MMGB's) [3] are formed which are "self-aligned" [2] to the edges of the gate electrode. It has been shown previously that in TFT's also employing self-aligned S/D doping, these MMGB's overlap the S/D metallurgical junctions and fall within the corresponding depletion regions, thus resulting in higher leakage current [4] and lower drain breakdown voltage [5]. In a comparative study [6] on the scaling behavior of SPC and MILC TFT's, it was shown that the latter scaled worse in terms of leakage current but better in terms of short-channel effects (SCE's). In this letter, the scaling behavior of the threshold voltage (V_{th}) at low drain voltage (V_d) is studied in detail. A reverse SCE (R-SCE) is reported in MILC TFT's and an explanation is given in terms of the overlap of the MMGB's and the S/D metallurgical junctions.

Manuscript received March 5, 1999; revised August 3, 1999.

The authors are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong.

Publisher Item Identifier S 0741-3106(99)08992-2.

II. Experimental

Four-inch silicon wafers covered with 100-nm thick thermal oxide were used as the starting substrates. A thin 100-nm amorphous silicon (a-Si) layer was first deposited by low-pressure chemical vapor deposition (LPCVD) at respective pressure and temperature of 300 mtorr and 550 °C. After patterning the a-Si layer to form the active islands, a 100-nm thick layer of LPCVD low-temperature oxide (LTO) gate insulator and 200-nm thick a-Si gate electrode were deposited. The wafers were thoroughly cleaned after the gate patterning and the exposure of the S/D regions. About 2 nm of Ni was evaporated in an ultrahigh vacuum system. Subsequently, the source, drain, and gate regions were doped by self-aligned 40 keV phosphorus implantation at a dose of $3 \times 10^{15}/\text{cm}^2$. The wafers were then heat-treated at 500 °C for 9 h, during which simultaneous Ni-induced crystallization of the a-Si layers and dopant activation were accomplished. Finally, contact holes were opened through 500 nm of LTO, Al-1%Si was sputter deposited. The devices were sintered in forming gas at 400 °C for 30 min. Hydrogen plasma passivation was performed in a 13.56 MHz parallel plate reactor at 300 °C in a 300 mTorr gas mixture of 200 sccm H_2 and 100 sccm N_2. The RF power was set at 250 W. A schematic cross section of the resulting MILC TFT is shown in Fig. 1(a).

III. Results and Discussion

Shown in Fig. 2 is a comparison of the channel length (L) dependence of the V_{th} of MILC and SPC TFT's, where V_{th} is defined as the V_g needed to achieve a drain current (I_d) of $W/L \times 10$ nA and W is the channel width. It can be observed that MILC TFT's are more resistant to SCE, since V_{th} roll-off occurs at $L \approx 5$ μm, which is quite a bit shorter than $L \approx 10$ μm for SPC TFT's. More interestingly, while the V_{th} of SPC TFT's decreases monotonically with L, that of MILC TFT's initially increases with L before rolling off at $L \approx 5$ μm, thus manifesting R-SCE.

R-SCE, due to defect enhanced lateral diffusion [7], [8], has been observed in scaled metal-oxide-semiconductor field-effect transistors (MOSFET's) realized on single-crystalline substrates. However, because of the transient nature of the underlying mechanism [8] and the resulting short diffusion length, R-SCE typically has been observed only in MOSFET's with submicrometer channel length. Both the initiation of the effect at a significantly longer channel length ($L > 20$ μm) and

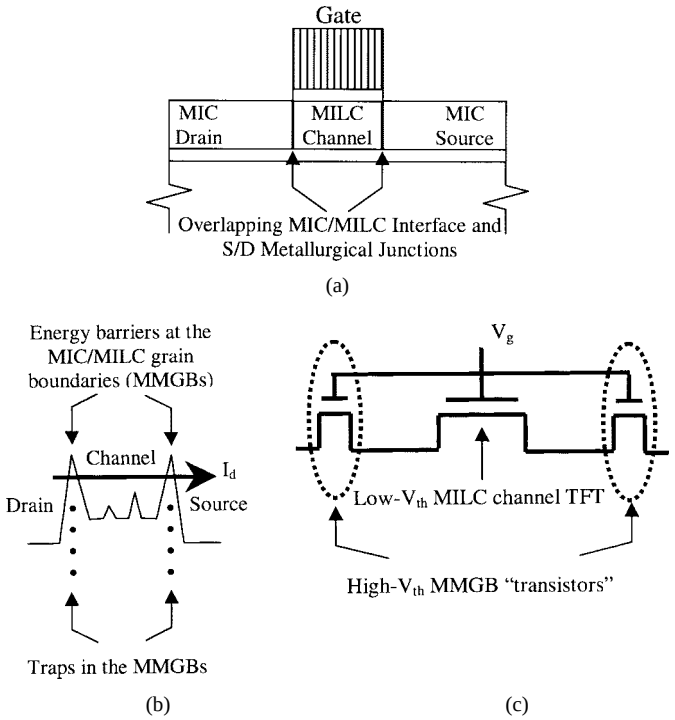

Fig. 1. (a) Schematic cross section of a conventional MILC TFT's showing the MMGB's self-aligned to the S/D metallurgical junctions, (b) the energy barriers near the metallurgical junctions of the source and drain, and (c) the device model at low V_d.

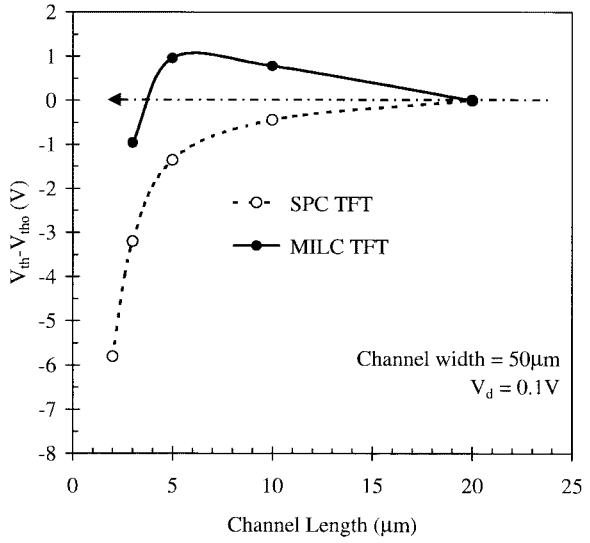

Fig. 2. Comparison of the V_{th} scaling behavior of MILC and SPC TFT's. R-SCE is evident in the MILC TFT's. Only changes in V_{th} are plotted, with V_{tho} denoting the threshold voltage measured on the transistors with the longest channel lengths.

the much lower device processing temperature makes it unlikely that transient enhanced diffusion is similarly responsible for the observed R-SCE in MILC TFT's.

On the other hand, because of the overlap of the MMGB's and the metallurgical junction regions at both ends of the channel, the MMGB traps are readily filled with charge carriers supplied by the source and drain. The resulting MMGB energy barriers, the height of which is a function of the trap densities,

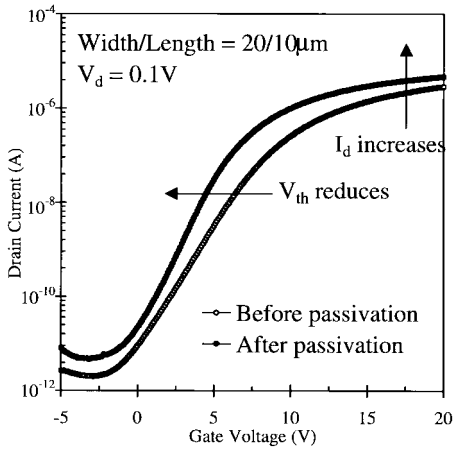

Fig. 3. Effects of plasma hydrogenation on the I_d–V_g characteristics of MILC TFT's, showing reductions in V_{th} and subthreshold swing.

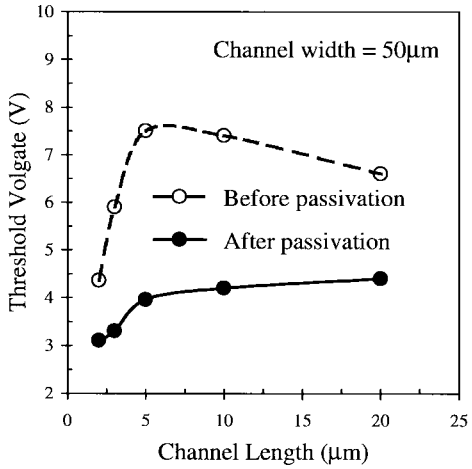

Fig. 4. Comparison of the V_{th} scaling behavior of MILC TFT's before and after hydrogen plasma passivation.

extend into the channel region. This is depicted in Fig. 1(b). Since a higher V_g is required to achieve surface inversion in the regions with the MMGB barriers, it is equivalent to adding two high-V_{th} MMGB "transistors," in series, to both sides of the intrinsic MILC transistor. This is depicted in Fig. 1(c). When L of the intrinsic MILC transistor is reduced, a larger fraction of the channel region comes under the influence of the MMGB energy barriers, thus raising the V_{th}. Further reduction of L leads to drain-induced barrier lowering (DIBL) and conventional SCE takes over, resulting in a reduction in V_{th} with L.

A consequence of this model is that if the density of the MMGB traps were reduced, the R-SCE would be reduced or eliminated. This can be accomplished by passivating the devices in a hydrogen plasma. Hydrogenation-induced reductions in both the V_{th} and the subthreshold swing can be observed in the I_d–V_g characteristics shown in Fig. 3. The data shown in Fig. 4 show that not only is V_{th} reduced because of the reduction of MMGB traps, the R-SCE is also eliminated after 30 min of hydrogenation.

IV. Conclusion

A reverse SCE is observed in conventional MILC TFT's with the MMGB's self-aligned to the source and drain metallurgical junction regions. A high potential barrier results from the MMGB traps, which leads to the observed reverse SCE. It is possible to reduce or eliminate the effect by reducing the density of MMGB traps. This can be accomplished by hydrogen plasma passivation.

References

[1] S. W. Lee and S. K. Joo, "Low temperature poly-Si thin film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.,* vol. 17, pp. 160–163, Apr. 1996.

[2] G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, "Effects of longitudinal grain boundaries on the performance of MILC-TFT's," *IEEE Electron Device Lett.,* vol. 20, pp. 97–99, Feb. 1999.

[3] Z. Jin, G. A. Bhat, M. Yeung, H. S. Kwok, and M.an Wong, "Nickel induced crystallization of amorphous silicon thin films," *J. Appl. Phys.,* vol. 84, no. 1, pp. 194–200, July 1, 1998.

[4] T. H. Ihn, B. I. Lee, T. K. Kim, K. H. Kim, J. W. Shin, P. S Ahn, W. C. Jeong, and S. K. Joo, "Fabrication of metal-gate poly-Si TFT's by metal-induced lateral crystallization," in *Dig. Tech. Papers, SID'97,* pp. 188–191.

[5] G. A. Bhat, M. Wong, Z. Jin, and H. S. Kwok, "Analysis and reduction of kink effect in MILC-TFT's," in *Proc. 18th Int. Display Research Conf.,* Seoul, Korea, Sept. 28–Oct. 1, 1998, pp. 433–436.

[6] G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, "Effect of MIC/MILC interface on the performance of MILC-TFT's," in *56th Annu. Device Research Conf.,* June 22–24, 1998, pp. 110–111.

[7] C. Y. Lu and J. M. Sung, "Reverse short-channel effects on threshold voltage in submicrometer salicide devices," *IEEE Electron Device Lett.,* vol. 10, pp. 446–448, Oct. 1989.

[8] K. Nishi, H. Matsuhashi, T. Ochiai, M. Kasai, and T. Nishikawa, "Evidence of channel profile modification due to implantation damage studied by a new method, and its implications to reverse short channel effects of nMOSFET's," in *IEDM Tech. Dig.,* 1995, pp. 993–995.