# High-Performance Polycrystalline SiGe Thin-Film Transistors Using $Al_2O_3$ Gate Insulators

Zhonghe Jin, Hoi S. Kwok, and Man Wong

***Abstract*—The use of aluminum oxide as the gate insulator for low temperature (600 °C) polycrystalline SiGe thin-film transistors (TFT's) has been studied. The aluminum oxide was sputtered from a pure aluminum target using a reactive $N_2O$ plasma. The composition of the deposited aluminum oxide was found to be almost stoichiometric (i.e., $Al_2O_3$), with a very small fraction of nitrogen incorporation. Even without any hydrogen passivation, good TFT performance was measured on devices with 50-nm-thick $Al_2O_3$ gate dielectric layers. Typically, a field effect mobility of 47 $cm^2$/Vs, a threshold voltage of 3 V, a subthreshold slope of 0.44 V/decade, and an on/off ratio above $3 \times 10^5$ at a drain voltage of 0.1 V can be obtained. These results indicate that the direct interface between the $Al_2O_3$ and the SiGe channel layer is sufficiently passivated to make $Al_2O_3$ a better alternative to grown or deposited $SiO_2$ for SiGe field effect devices.**

***Index Terms*—Aluminum oxide, displays, insulator, interface, polycrystalline silicon-germanium alloys, thin film transistors.**

## I. Introduction

IT HAS been proposed that SiGe is an attractive alternative to Si in a variety of micro-electronic applications. In bipolar transistors, it has been used to form narrow bandgap base regions [1]. In field effect devices, it has been used to form variable workfunction gate electrodes [2]. In large-area electronics such as flat panel displays, its advantages include lower solid-state crystallization temperature and potentially higher mobility [3]. In all of these applications, the processing of SiGe is believed to be "compatible" to the processing of Si. However, because of the poor interface between a conventional $SiO_2$ gate insulator and the polycrystalline SiGe (poly-SiGe) channel layer, there is still significant disparity, particularly for NMOS thin-film transistors (TFT's), between the best reported performance of poly-SiGe and that of poly-Si TFT's, even after extensive optimization [4], [5]. Clearly, improving the quality of the interface, rather than that of the channel layer, holds the key to realizing better performing poly-SiGe TFT's.

Various techniques of improving the interface quality, including alternative methods of gate oxide formation [6], [7] or the insertion of an Si buffer layer [8], have been investigated with some degrees of success. Recently, excellent device performance has been reported [9] on Si-buffered poly-SiGe TFT's with $Al_2O_3$ as the gate insulator. In this work, the performance of TFT's with a direct $Al_2O_3$/SiGe interface has been investigated.

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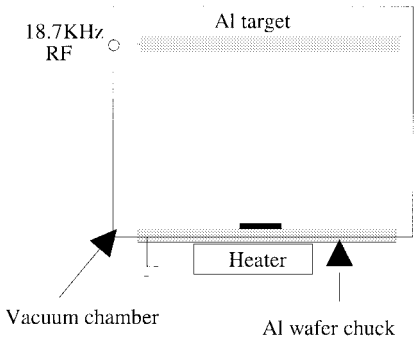


Fig. 1. Schematic diagram of the reactive sputter deposition system.

## II. Experimental

The $Al_2O_3$ thin films in this work were deposited in a novel RF plasma reactive sputtering system, schematically shown in Fig. 1. The pure Al target and the wafer chuck form the parallel plate electrodes for the reactive $N_2O$ plasma. The diameters of the target and the wafer chuck are about 5 cm. The wafer temperature, the process pressure, the $N_2O$ flow rate, and the power of the 18.7-kHz RF power were 380 °C, 200 mtorr, 400 sccm, and 450 W, respectively. The resulting deposition rate was about 0.6 nm/min.

X-ray photo-electron spectroscopic (XPS) depth profiles of the atomic concentrations of various elements within an as-sputtered film are shown in Fig. 2. The thickness of the film is about 50 nm, with a ratio of aluminum to oxygen around two to three, and a small but nonnegligible nitrogen content. This indicates that the film is largely stoichiometric $Al_2O_3$. The 76.4-eV Al2p binding energy determined using XPS provides further proof of the full oxidation of Al.

NMOS poly-SiGe TFT's were fabricated using a four-mask self-aligned process. Starting with 100 mm, (100)-oriented N-type Si wafers with 500 nm of thermally grown oxide, a 100-nm-thick layer of SiGe was deposited at 550 °C in a low pressure chemical vapor deposition (LPCVD) system [10] to form the channel layer. Silane and germane at respective flow rates of 100 and 10 sccm were used as the source gases. The Ge content in the deposited SiGe films was 15%, determined using Rutherford backscattering spectroscopy. X-

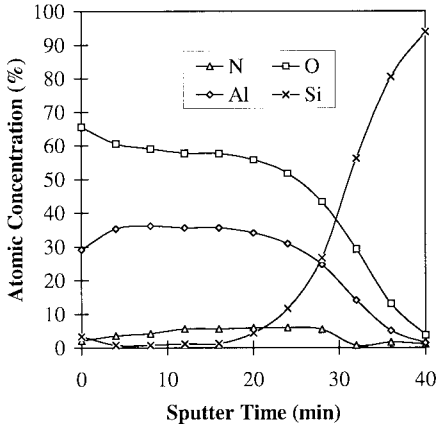


Fig. 2. XPS depth profile of $Al_2O_3$, as-deposited on crystalline silicon.

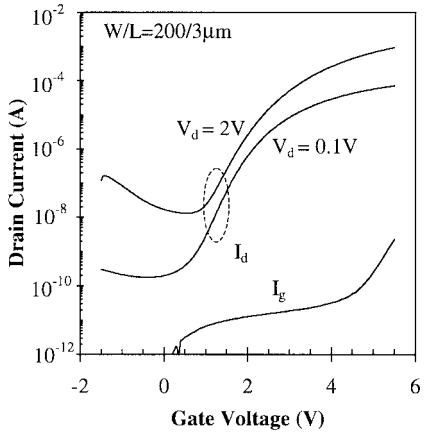


Fig. 3. $I_d$–$V_g$ curves and gate leakage current of the poly-SiGe TFT with 50-nm $Al_2O_3$ gate insulator.

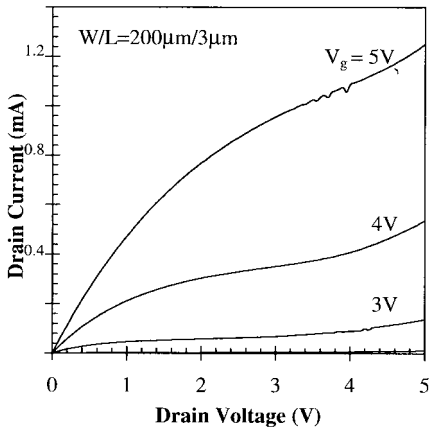


Fig. 4. $I_d$–$V_d$ curve of the poly-SiGe TFT with 50-nm $Al_2O_3$ gate insulator.

ray diffraction analyses indicated that the as-deposited films were polycrystalline. Following the channel island patterning by plasma etching, the wafers were cleaned and loaded in the reactive sputtering system for the $Al_2O_3$ dielectric deposition. The thickness of the film was adjusted by controlling the deposition time and checked using a surface profilometer. The gate electrodes were realized by patterning 280-nm-thick LPCVD $Si_{0.55}Ge_{0.45}$ thin films. Any $Al_2O_3$ not covered by the gate electrode was etched in a buffered HF solution, and doping was accomplished by a self-aligned $4\times 10^{15}/cm^2$ phosphorus implantation. Before the 5-h implant activation at 600 °C, a 500-nm-thick CVD low-temperature oxide (LTO) pre-metal insulation layer was laid down, using $SiH_4$ and $O_2$ at 425 °C. Subsequently, contact holes were opened in a buffered HF solution and 1 $\mu$m of Al-1%Si was sputter deposited. Finally, the devices were sintered in Forming gas for 30 min at 400 °C. No deliberate hydrogenation was performed, so that the "intrinsic" performance of the devices can be measured.

## III. Results and Discussions

The fabricated devices were characterized using an HP4156 Precision Semiconductor Parameter Analyzer. Typical room-temperature IV curves of the poly-$Si_{0.85}Ge_{0.15}$ TFT's and the corresponding gate leakage current are shown in Fig. 3. Though the gate current begins to increase softly at around 4.5 V, it is low during all the measurements. Such gate leakage can be reduced by optimizing the deposition and the annealing condition of the reactively sputtered $Al_2O_3$ film or by capping it with a thin layer of LTO. The drain current $(I_d)$ begins to increase rapidly at a gate voltage $(V_g)$ of 1 V and enters the linear regime at about 3 V—indicating a very effective gate control. The estimated threshold voltage and the subthreshold slope are 3 V and 0.44 V/decade, respectively. At a drain voltage $(V_d)$ of 0.1 V, the off current is lower than 1 pA/$\mu$m. This translates to an on/off ratio of greater than $3\times 10^5$, even without any deliberate hydrogen passivation. An electron field-effect mobility $(\mu_{\rm FE})$ of 47 $cm^2$/Vs can be estimated using the following equation:

$$\mu_{\rm FE}=\frac{1}{C_{\rm ox}}\left(\frac{L}{W}\right)\frac{1}{V_d}\frac{dI_d}{dV_g}$$

where $L$ is the channel length, $W$ the channel width, and $C_{\rm ox}$ the capacitance per unit area of the 50-nm $Al_2O_3$. A relative dielectric constant of ten was assumed for $Al_2O_3$. This mobility is much better than that of the hydrogenated poly-SiGe TFT's using $SiO_2$ as the gate insulators [3]–[5].

A set of $I_d$–$V_d$ curves is shown in Fig. 4. The behavior is typical of field effect TFT's showing partial saturation effects at high $V_d$. The slight increase of $I_d$ at $V_d$ above 4.5 V is probably caused by grain boundary enhanced "kink" effects [11].

The performance of the device shown in Figs. 3 and 4 is much better than similar devices with $SiO_2$ as the gate insulators. A comparison of the relevant parameters is summarized in Table I. The good subthreshold slope obtained in this work is better than those obtained from heavily hydrogenated devices with $SiO_2$ gate insulators, with or without an Si buffer. Part of this improvement resulted from the higher relative dielectric constant of $Al_2O_3$, which is about 2.5 times that of $SiO_2$. A more important reason is the improved interface between the $Al_2O_3$ dielectric and the SiGe channel layer. The mobility obtained in this work is comparable to state-of-the-art poly-Si devices. This is the first time ever that high mobility poly-SiGe TFT's have been realized without extensive hydrogenation.

TABLE I
COMPARISON OF NMOS POLY-SiGe TFT's WITH $Al_2O_3$ OR $SiO_2$ AS GATE INSULATOR.

| | Without Hydrogenation | With Plasma Hydrogenation | | |
|---|---|---|---|---|
| Gate insulator | $Al_2O_3$ (50nm) | $SiO_2$ [a] (100nm) | $SiO_2$ [b] (100nm) | $SiO_2$ [c] (100nm) |
| $\mu_{FE}$ ($cm^2/Vs$) | 47 | 28 | 38 | ~35 |
| Threshold voltage (V) | 3 | 8 | 5.5 | ~8 |
| Sub-threshold slope (V/decade) | 0.44 | 1.6 | 1.5 | ~2 |
| On/off ratio | $3x10^5$ (@ $V_d$ = 0.1V) | Not extracted | $\sim 2x10^5$ (@ $V_d$ = 10V) | $\sim 1x10^6$ (@ $V_d$ = 10V) |

a. Ref. 4: SPC $Si_{0.88}Ge_{0.12}$.
b. Ref. 5: SPC $Si_{0.83}Ge_{0.17}$.
c. Ref. 8: SPC $Si_{0.8}Ge_{0.2}$ with 20nm Si buffer.

This makes $Al_2O_3$ a significantly better substitute for $SiO_2$ as the gate insulators for poly-SiGe TFT's.

As shown in Fig. 2, the deposited $Al_2O_3$ film typically contains about 5% nitrogen. This is because $N_2O$ was used as the reaction gas instead of pure $O_2$. At the present moment, it is not clear if the nitrogen plays an active role in improving the interface quality. Experiments are planned to clarify this ambiguity and to improve the breakdown voltage of the material.

## IV. CONCLUSION

A novel reactive sputter deposition system was used to form $Al_2O_3$ as the gate insulators of poly-SiGe TFT's. Material analyses indicate the deposited film is largely stoichiometric $Al_2O_3$, with about 5% nitrogen incorporation. Devices fabricated with the $Al_2O_3$ gate insulators showed excellent performance even without any deliberate hydrogenation. Compared to poly-SiGe TFT's with $SiO_2$ as gate insulators, the field-effect mobility and the subthreshold slope improved significantly, indicating a good direct interface between the $Al_2O_3$ gate insulator and the SiGe channel layer. These results suggest that $Al_2O_3$ is more suitable than $SiO_2$ as a gate insulator material for poly-SiGe TFT's.

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